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Guidelines for Space Qualification of GaN HEMT Technologies

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John R. Scarpulla[1] and Caroline M. Gee[2]
[1]Electronics Engineering Subdivision, Electronics and Sensors Subdivision
[2]Microelectronics Technology Department, Electronics and Photonics Laboratory

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This set of guidelines had its inception in some presentations by the authors given to various space organizations answering the question: “How might GaN HEMTs be space qualified?” Later a draft set of guidelines was prepared and circulated more widely. In the latter half of 2019, weekly telecon meetings were held with a group of interested parties from government, industry, semiconductor fabrication houses, universities, and aerospace contractors. This group of people made many contributions to mature the original draft. Their help is gratefully acknowledged. Many useful comments and suggestions were made to greatly improve the scope and relevance of this guideline. We acknowledge the contributors listed below.

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Assad, Chahriar Ph.D.
Technical Fellow
The Boeing Company

Bole, Kenneth
Senior Research Engineer
Air Force Research Laboratory
Kirtland AFB, NM

Boutros, Karim Ph.D.
Senior Technology Qualification Engineer
Boeing

Buttari, Dario
Staff Engr Microelec Smcndctr
Northrop Grumman

Cantarini, Bill
Founder
HiRel Component Solutions, LLC

Carlos, Zenon F.
Component Engineer–RF Devices
Boeing Research and Technology

Cole, Everett
Director of Manufacturing; Aerospace and Defense
Analog Devices Inc.

Cox, Bill
Sr. Component Engineer
Maxar

Decker, Ken
Director of TX Advanced Reliability
Qorvo

de Leon, Rodrigo
Boeing Associate Technical Fellow, Electrical PM&P
Boeing Research & Technology, MTI-Defense & Space

Drandova, Gergana Ph.D.
Senior Member Technical Staff, Research
Qorvo

Ejeckam, Felix
CEO and Co-Founder
Akash Systems, Inc.

Eng, David
Manager, Microelectronics Reliability
Northrop Grumman

Ersland, Peter
Reliability Engineer
MACOM Technology Solutions

Ganguly, Satyaki Ph.D.
Reliability Scientist
CREE | Wolfspeed

Han, K. Michael
Senior Specialist
Jet Propulsion Laboratory, California Institute of Technology

Harzstark, Larry
Aerospace Fellow
The Aerospace Corporation

Heller, Eric Ph.D.
Research Physicist
Materials and Manufacturing Directorate, Air Force Research Laboratory

Hummel, Martin
Component Engineer, SoCal M&P
Boeing Research and Technology

Ihsan, M. Amimul
RF Engineer Sr. Staff
Lockheed Martin Space

Jung, Thomas Ph.D.
Senior Project Engineer
The Aerospace Corporation

Kasim, Kawthar
Thermal Analyst
Boeing

Lauenstein, Jean-Marie Ph.D.
Aerospace Engineer
NASA GSFC

Lee, Timothy
Boeing Technical Fellow
Boeing

Lodhi, Tariq
MMIC Engineer
Analog Devices Inc.

Mayberry, Clay
Senior Engineer
Air Force Research Laboratory/RVBYS

Mongia, Rajesh
Director, MMIC Engineering
ENGIN-IC

Ohoka, Mikiharu
Sr. Director, MW Sales, Marketing and Engineering
Sumitomo Electric Device Innovations USA, Inc.

Osheroff, Jason
Radiation Engineer
Science Systems Applications, Inc.

Peterson, George Ph.D.
Research Associate
Air Force Institute of Technology

Poling, Brian
Electrical Engineer
Air Force Research Laboratory

Quinlan, Jeanette
Director of Space Systems
Akash Systems, Inc.

Schwartz, Stanley
Principal Engineer
Lockheed Martin Space

Smith, Phil
Sr. Manager, Components Engineering
L3Harris

Sullivan, Dan
Director–Sales & Marketing
KCB Solutions

Thomas, Stephen III
Associate Technical Fellow
Boeing Space and Launch

Torabi, Abbas
Sr. Principal Engineer
Raytheon

Wang, Dave S. K.
Chief Technology Officer
Global Communication Semiconductors, LLC

Xiong, Shunhe
Principal Packaging Engineer
IR HiRel, An Infineon Technologies Company

Ying, Helen
Manager, Space Parts Management
Raytheon, Space and Airborne Systems

Zygmaniak, Jan J.
Sr. Manager, RF Engineering
L3Harris Technologies

Foreword

GaN HEMT technology has now been in commercial development for about a decade and a half and has matured to a high level. It has begun to replace other technologies used in SSPAs (solid-state power amplifiers), such as GaAs pHEMTs and Si LDMOS (laterally diffused metal-oxide semiconductor) technologies. It has decided performance advantages, including its power capability, and thermal factors. It is even beginning to supplant the TWTA (traveling wave tube amplifier) in high-power applications. However, at this time it has not been used in a Class A or Class B space mission.

The GaN technology differs from other semiconductor technologies in many ways. Existing qualification standards are not fully compatible with its properties. There is has been a growing question about exactly how to qualify a GaN technology for a space mission. The writing of this document evolved from that need.

The objectives envisioned for this document are twofold. The first objective is to recommend procedures and tests for the qualification of RF (radio frequency) and microwave GaN HEMTs and HEMT-based MMICs for space missions. This document is not a specification or a list of requirements. Rather, it is a set of recommendations that can be tailored to a space mission application. The second objective is to provide background and rationale for the recommendations themselves. Many semiconductor device performance requirements, source control drawings, military standards, and procurement documents are often prescriptive in nature. They do not normally provide the reasons behind the various and sundry tests that they require. GaN HEMT technology is a relative newcomer to the high-reliability space enterprise, and the technology differs in many ways from other semiconductor technologies (such as Si CMOS or GaAs HEMT technology). It was therefore recognized that the existing test methods and techniques employed to qualify Si or GaAs devices were not necessarily adequate or complete for GaN HEMTs and MMICs. To that end, many new and specific tests and procedures are recommended in this guideline that are unique to the GaN HEMT technology. Many have no analog in Si or GaAs. This guideline contains example data, explanations of test objectives, methods of analysis of test data and reliability calculation examples. References have been provided for further background and information. This guideline is not a specification but rather provides a set of approaches recommended to aid in space qualification of GaN HEMTs for a particular space mission. These recommendations should always be tailored as needed.

Success in the space environment is difficult because of the myriad of unfamiliar nonterrestrial characteristics—temperature cycling between extremes, ionizing radiation, shock and vibration of launch, long mission durations, operation in vacuum, and others. Added to these characteristics is the constant push for higher and higher payload performance—RF output power, efficiency, SWAP (size, weight, and power) constraints, low phase noise, high-frequency stability, linearity, dynamic range and more. GaN HEMTs excel in many of these areas. It is hoped that if the recommendations in this guideline are followed, these advantages can be fully realized in space missions. The qualification tests and methods identified herein are intended to address the unique aspects of GaN HEMT technology.

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1. Introduction

The properties of the GaN HEMT technology make it especially attractive for many high-reliability space applications and missions, especially in the areas of communications, sensors, power amplifiers, and radars. The combination of its ability to operate at high temperature, to be capable of supporting high voltage, and handling a high current density are properties that are particularly valuable. Commercial products have been developed that exploit these properties and perform useful functions. The open question at this time is whether the GaN technology will be sufficiently reliable for the long term and hazardous space missions to which it could be well suited. U.S. military missions are long, measured in years or decades, and the space environment is challenging with temperature extremes, vibration, and ionizing radiation(s). It is believed that with adequate testing and evaluation on the ground, it will be possible to recommend GaN technologies for high-reliability space missions.

At the time of this writing, there are two GaN HEMT experiments flying in satellites. They are both small X-band transmitters—one in the ESA Proba V satellite, launched in May 2013, and the other in the JAXA Hodoyoshi-4 satellite, launched in June 2014. Neither one is representative of the U.S. military Class A or B missions (as defined in Johnson-Roth, 2011) having long duration, high reliability, complexity and other demanding attributes. In its present state, the United States GaN HEMT space technology is believed to be at TRL 4–5 (Technology Readiness Level) per the DOD guidelines (US-DoD TRL 2011). It is our hope that the recommendations in this document will help to elevate the technology readiness level to TRL 6 and beyond.

The purpose of this document is to set forth recommended tests and test protocols that will enable GaN semiconductor technologies to become qualified for use in U.S. DOD (Department of Defense) and NSS (national security space) space applications of Class A or B. GaN is a new technology that has been in development for approximately 20 years. Useful applications for this technology are in the areas of RF/microwave transistors and MMICs, especially for higher-power applications. The GaN technologies are also being applied to power conversion and power-switching applications. This document addresses only the former set of applications—RF/microwave uses of GaN. The power supply applications are sufficiently different to warrant a somewhat different set of qualification tests and are not addressed here. These considerations will possibly be addressed in a future revision. Furthermore, the express purpose of this document is to address conventional AlGaN/GaN HEMTs or HEMT-like devices (having a metal Schottky barrier gate) or similarly based MMICs. The substrates may be SiC, Si, sapphire, native GaN, or other substrates. Newer MIS- (metal insulator semiconductor) HEMTs or IG- (insulated gate) HEMTs are specifically not included herein. These devices have not yet achieved mainstream status for high-reliability applications. This situation is rapidly changing, and an update to this document may be needed soon. These newer HEMT technologies have sufficiently different qualification concerns especially related to the reliability of the gate insulator. These concerns are not addressed in this document.

The GaN HEMT technology encompasses power transistors (microwave HEMTs) and full MMICs that differ in the degree of integration of multiple device types. In the power transistors, the devices are large–gate width HEMTs and sometimes include matching components, such as MIMCAPs and inductive bond wires as part of the packaging. These components must be qualified in addition to the GaN HEMT device itself. The device package plays a major role in the reliability and is important to consider as part of the space qualification. On the other hand, power transistors in the form of die that are to be packaged in hybrids or other microwave components by the user require different considerations for qualification. Lastly, in the case of MMICs, the GaN technology includes many other constituents, such as multilayer metals and dielectrics, MIMCAPs, backside vias, thin film resistors, and other features. They must be qualified for their reliability as individual components of the fabrication process. Toward that end, process control monitoring (PCM) and statistical process control (SPC) are highly recommended methods

in the total fabrication processing of GaN devices, or for that matter any semiconductor process technology. The topic of efficient test structures, PCMs, and measurement techniques is beyond the scope of this document but deserves more attention. The purpose of the present document is to recommend qualification tests and procedures for completed HEMTs and MMICs that are "finished goods" that can be directly utilized as purchased parts in a spaceworthy subsystem. This guideline is intended as an aid to developing a process qualification plan for GaN semiconductor device manufacturing line or for a particular GaN product and mission.

1.1 Considerations for GaN HEMT Space Qualification

GaN is a compound semiconductor that ostensibly appears to be similar in many ways to its main predecessor GaAs technology. There are many similarities. However, GaN is uniquely suited to high-power applications that are beyond the domain of the GaAs technologies. The realm of high-power RF/microwave operation requires a different set of considerations for qualifying the technology for space. It is important to understand the differences and to properly account for them. It would be a mistake to simply perform the same tests on GaN devices that have enabled previous space qualification of GaAs devices. The failure mechanisms and methods of acceleration of these failures are now known to be different between the technologies. It is important to understand these mechanisms for space qualification of the GaN technologies.

In mature semiconductor technologies such as Si and GaAs, one of the most important milestones in qualification of a device or fabrication line is the HTOL (high temperature operating life). In this test the device is operated at DC or sometimes with RF or pulsed RF and is subjected to 1000 hours of elevated ambient temperature, typically 125 °C or 150 °C, accompanied usually by a much higher channel temperature. Then afterwards, the devices are tested and the number of failures determined. Often this number is zero. Then using a series of assumptions, the failure rate can be computed. The assumptions are:

- It has a single dominant failure mechanism.
- It has a known activation energy (typically 0.7 eV or 1 eV).
- It has a constant failure rate, equivalent to an exponential cumulative failure distribution.
- The failure rate is then determinable using a chi-square distribution.
- It has a constant usage channel temperature of 105 °C (sometimes more or less).

While this approach works well for mature semiconductor technologies, it is not appropriate for new technologies where these assumptions are not valid or not yet proven. For GaN HEMT devices, the failure rates are not constant, the activation energies are not necessarily known, and there may be more than one failure mechanism. A different approach is needed for establishing the reliability for stringent long-duration, high-reliability space missions.

Figure 1-1 is an attempt (perhaps in exaggerated fashion) to show some of the failure mechanisms that may exist in a GaN HEMT (Heller, 2012; Cheney, 2012; Meneghesso, 2008; Zanoni, 2017). A brief and partial list of these failure modes is as follows:

- Surface pitting or erosion at the gate-drain edge creating cracks or voids. Surface pitting may be the result of piezoelectric strain at the high field point at the gate-drain edge. It reduces the drain current. (Makaram, 2010; Sun, 2014; Paine, 2017a). Pitting also may be the result of corrosion caused by an electrochemical reaction in the presence of moisture (Gao, 2014).

- Trap generation in the AlGaN barrier layer at the gate-drain edge caused by hot electrons when the drain voltage exceeds a critical value. The traps introduce time dependent "current collapse" and a possible percolation gate leakage component (del Alamo, 2009; Marcon, 2013).

- Hot electron injection into the passivation or the AlGaN barrier layer in the drain access region, creating a "virtual gate" accompanied by drain lag and degradation in gain and drain current (del Alamo, 2009; Heller, 2014).

- Creation of the virtual gate by charging of existing surface trap states in the AlGaN barrier layer (Vetury, 2001), or creation of new traps and dislocations (Ramanan, 2014). The virtual gate is located in the drain-gate access region. The traps and dislocations cause undesirable threshold shifts and increased on-state resistance.

- Creation of a similar virtual gate by virtue of leakage of electrons from the gate into the AlGaN layer trapping in the AlGaN and creating new traps. The mechanism of leakage current may be Fowler-Nordheim tunneling, Frenkel-Poole conduction, or hopping transport (Ghosh, 2018). Leakage is enhanced at the drain edge of the gate with elevated drain voltage. The virtual gate increases the parasitic drain access resistance and causes undesirable threshold shifts.

- Gradual time-dependent degradation of gain or output power, and gradual shift of threshold voltage with operation above a certain "critical" drain voltage (Joh, 2008; Wang, 2012). This critical voltage may be a dividing line between different failure modes in a GaN HEMT.

- Contact resistance degradation at the source/drain contacts due to interdiffusion, voiding, or reactions (Wua, 2014; Piazza, 2009)

- Schottky gate contact degradation, especially under forward bias (Axelsson, 2015)

- Source via degradation, voiding or increased ohmic resistance

- Field plate dielectric time-dependent dielectric breakdown (TDDB)

- Degradation of the thermal boundary resistance existing at the interface between the substrate and the GaN layer (Manoi, 2010)

- Hydrogen poisoning, especially with Ti with Pt, or Pd in the gate stack, causing possible threshold shifts, and increased sensitivity to hot electrons (He, 2019)

- Diffusion processes along crystal dislocations generating traps in the AlGaN barrier layer (Kuball, 2011)

- Migration of gate metal leading to open voiding failures, believed to be driven by electromigration and/or stress gradients (Paine, 2017b)

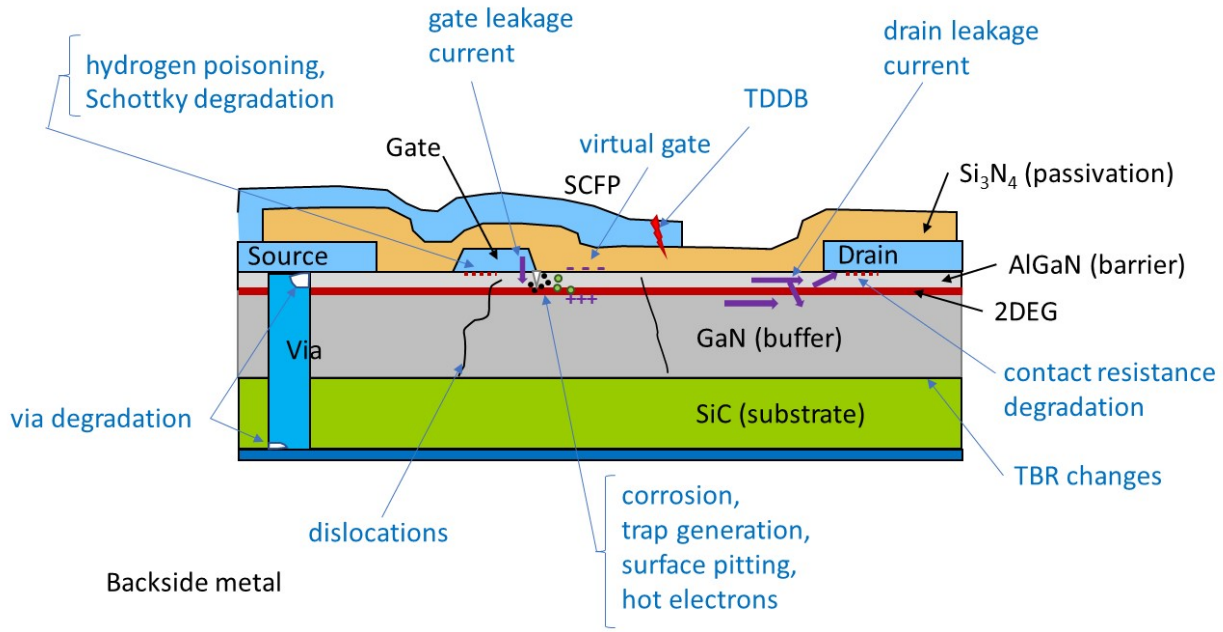


Figure 1-1. Cross section of a typical HEMT, identifying some of its failure mechanisms (current arrows denote electron currents.).

Many of these failure mechanisms are not necessarily thermally activated but rather electric field driven or piezoelectrically driven. Furthermore, it is not certain which, if any are dominant in any particular usage application. An approach that has been largely successful in the past for GaAs MMIC and HEMT technology qualification is based upon an existing specification for GaAs accelerated temperature lifetesting (JEDEC standard JEP118A). Here the use of multiple temperature lifetests of varying durations are specified toward the aim of obtaining (as well as assuming) a single activation energy. This is a perfectly serviceable approach provided that the assumption of a single dominant failure mechanism is valid. Since the main circuit application of GaAs has been for LNAs (low-noise amplifiers) that operate essentially under small signal Class A conditions, the assumption usually has been valid. The dominant failure mode in GaAs LNAs is gate sinking, which gradually reduces the gain, drain current, etc. However, even in GaAs power amplifiers, it is well known that there are multiple failure modes, such as hot electron degradation and ohmic contact degradation to name a few. Now the assumption of a constant single thermal activation energy useful to predict reliability is no longer valid, and the methods of JEP118A are no longer as useful. We are faced with a similar situation now with the GaN technologies, where the major circuit applications are power amplifiers rather than LNAs. The single dominant failure mode assumption is generally invalid for GaN RF power transistors and MMICs. This suggests that thermal acceleration of failure alone is not necessarily the best method for the determination of GaN HEMT reliability (Chini, 2012; Paine, 2015c; Coutu, 2016; Burnham, 2017). It suggests that among others, voltage is an important accelerant of failure in GaN devices. In fact, a portion of this guideline is devoted to the assessment of the reliability under high-voltage, low-current conditions, and off-state conditions. Another portion describes the existence and determination of a “critical voltage” in GaN HEMTs where voltage-driven (rather than temperature-driven) reliability failure modes begin to manifest themselves. This is quite different than what is found in GaAs HEMTs.

A property of GaN HEMT technology is the prevalence of electronic traps. Because of the lattice mismatch between the typical Si or SiC substrate and the deposited GaN and AlGaN epitaxial layers, a mechanical strain exists in the epi layers. This strain leads to epi layer defects such as misfit dislocations, threading dislocations, slip planes, etc. Each of these types of crystal defects can cause trapping of charge carriers. The effect in GaN HEMTs is rather pronounced as compared to GaAs pHEMTs. A comparison

of static IV versus pulsed IV characteristics of a typical GaN microwave HEMT readily reveals the effects of trapping. The pulsed IV curves usually are quite different from the static IV curves. The reason is that the trapping phenomena are time dependent so that the number of filled versus empty traps is constantly changing according to the time-varying applied voltage, and RF signals. In essence, a GaN microwave HEMT is not a fixed device but rather has dynamic behaviors that must be taken into account. Some terms used to describe these effects are current collapse, gate-lag, drain-lag, frequency dispersion, pulse-to-pulse instability, etc. Despite these phenomena, GaN HEMTs or MMICs still offer excellent performance in many applications. It is important that the presence of these dynamical effects do not affect long-term reliability in a typical space mission.

Many if not most RF and microwave signals in space systems are pulsed in nature. The GaN HEMT trapping phenomena may give unexpected results in pulsed applications. A major advantage of a GaN RF power device is of course its high power capability—as a combination of its high current capacity per unit device width, high-voltage capability, and tolerance for high temperature operation. However, a disadvantage may well be that the trapping effects cause pulse instabilities (Tome, 2019). For example, the output power may be time dependent and/or dependent on pulsewidth. Pulse-to-pulse variability may exist. Power output is a function of the state of trapping, which in turn may be a function of the previous history of electrical signals and bias. Gate and drain lag phenomena are a form of hysteresis that may cause problems in some applications. Trapping may worsen with stress, aging, and space radiation. At this time there is no industry standard way to capture the reliability implications of the traps in GaN HEMTs. In this sense, GaN HEMTs are quite different from GaAs HEMTs. This difference should be kept in mind when utilizing or qualifying GaN HEMTs and MMICs for space missions. Some measurement techniques that are sensitive to the trapping phenomena are proposed in Section 3. They are quite different from the essentially static measurements that are sufficient to qualify GaAs devices space applications.

In the following paragraphs some suggestions are provided to qualify GaN HEMT technologies for reliable operation in space missions. The topics include various tests for electrical robustness, intrinsic failure modes, environmental factors, extrinsic components (such as MIMCAPs), mechanical integrity, and radiation effects. It is our intent to propose or recommend test methods appropriate for Class A or B missions. As with any set of qualification methodologies, tailoring of the recommendations is always necessary for a particular mission or usage requirement. It is safe to say that not all tests would be required for all missions. An appropriate PMPCB (parts, materials, and processes control board) or other governing body should be designated for tailoring these recommendations for a particular program.

This document is divided into the following sections:

1. Introductory (this section)
2. Tests for Basic Electrical Robustness
3. HEMT Reliability Tests for Intrinsic Failure Modes
4. Qualification for Environmental Factors
5. Qualification for Extrinsic (Defect Related) Failure Modes
6. Qualification for Mechanical Integrity & Packaging
7. Radiation Tests
8. Open Issues and Recommended Work
9. Fifty Questions to Ask Your GaN HEMT or MMIC Supplier

In each area, a series of recommended tests is proposed. A checklist of all the tests is shown in Appendix A and includes the purpose, the DUT (device under test) quantities, number of sample lots, environmental specifics, and the success criteria for each. Appendix B provides a list of external specifications and standards referenced herein. Appendix C lists acronyms used in this document. Appendix D is a

discussion of ratings and deratings for GaN HEMT devices. Appendix E covers the specialized area of temperature measurements for GaN devices. Appendix F shows how to compute the reliability of MIMCAPs, and Appendix G provides some additional information about radiation effects in GaN, particularly dose in Rads(GaN) as compared to Rads(Si), dose enhancement in GaN, and a comparison of displacement damage in GaN versus Si. Finally, Appendix H provides a computation of the maximum permissible drain voltage for a given reliability requirement, and Appendix I contains references.

1.2 DUTs, Configurations, Quantities, and Test Frequencies

In any process or product qualification, many samples of the devices or structures of interest must be subjected to stress testing, mostly (but not always) in accelerated fashion. DUTs (devices under test) in sufficient quantities must be devoted to each failure mode to achieve reliability goals. In the following sections, specific DUT quantity recommendations are provided, along with their recommended configuration. In some cases, a full flightlike configuration—for example, a hermetic package—is required. In other cases, a more convenient nonhermetic package, an open fixture, a wafer, or a specific test structure is recommended. It also may be possible to perform many of the tests at wafer level.

A one-line table is provided in each section below containing the recommended DUT and lot quantities, DUT configuration, and test frequency. The DUT quantities are patterned loosely after the recommendations of JEP118A, which specifies 50 devices for a 3TLT (three-temperature lifetest). Many of the GaN qual tests recommended below require additional bias points or more test conditions. So as to obtain reasonable statistical parity with JEP118A, the device quantities in this document have been chosen. Quantities may need to be increased or decreased for various reasons. For example, for a small fab house, these quantities may be unnecessary if a single product die or MMIC is under consideration. The qualification then would be limited and would not encompass other products from that line. For a larger fab, there may be a need to increase DUT quantities to encompass process variations, different substrates or starting materials or different backside processing. The main intent of this document is to recommend a set of tests to arrive at a space-qualified GaN process that may applied to any product die or MMIC from the line. Reduced quantities may be appropriate with a reduced scope of qualification.

Many of the tests recommended in what follows are one-time tests only, to be performed at the outset of a qualification. It should be recognized that fabrication processes are always under a state of flux, with different pieces of equipment and process adjustments made on a continual basis. When changes merit the need for requalification, the tests recommended here should be repeated. A TRB (technology review board) is needed to make this determination, as stated in Appendix C of MIL-PRF-19500P.

2. Tests for Basic Electrical Robustness

The following paragraphs define some basic tests needed to qualify the electrical limits in GaN discrete HEMTs and the active devices within GaN MMICs. Firstly, it is important to distinguish between the various types of imposed maximum specification limits and operating conditions that are placed on GaN RF and microwave devices. These limits in order of increasing magnitude or intensity are:

- DC Q-point (quiescent point or operating voltage)
- SOA (safe operating area; sometimes with an implicit derating factor)
  - drain SOA
  - gate SOA
- Critical Voltage
- Maximum Safe Voltage Ratings
- RF Survivability Limit
- Catastrophic Breakdown Voltage

A brief discussion of these limits is found in Appendix D. (The use of the term "absolute maximum" is specifically avoided here since the term has many meanings). Unfortunately, there is no industry standard that exists for specification of these limits on manufacturers' data sheets. In general terms, the SOA appropriate for GaN devices is defined here as the region in IV space (whether for drain or gate) where the device may be operated in DC or pulsed fashion with no expectation of catastrophic failure. However, that is not to say that there might be some gradual degradation with extended operation in certain portions of the SOA. For this reason, reliability assessments must also be conducted as described in Section 3. The SOA is intended to cover the regime of normal operation, albeit with some wearout failure occurring late in life—much later than the mission requires. Based upon Appendix D, it is recommended that the following definitions be utilized for high-reliability space applications of GaN HEMTs and MMICs.

Definitions

- Maximum safe drain-source voltage $V_{DSmax.safe}$ refers to the maximum safe peak instantaneous voltage under any condition (DC or peak RF). The catastrophic drain breakdown voltage shall be 2–3× higher than $V_{DSmax.safe}$. The value of $V_{DSmax.safe}$ may be constrained further by intrinsic reliability requirements (see Section 3 and Appendix H), or by single-event effects, SEE (see Section 7 and Appendix G).

- A drain SOA (safe operating area) whether DC or pulsed refers to the regions in the I_D vs. V_{DS} plane for which no catastrophic damage, reliability degradation or SEE ensues. The drain SOA is a combination of dissipated thermal (power) $P_{diss.max.safe}$, voltage $V_{DSmax.safe}$, and current $I_{Dmax.safe}$ limits. The drain SOA may be extended for pulsed operation based upon temperature rise allowable. Operation at the extremes of the SOA, while not catastrophic, may still incur gradual degradations. Reliability assessments are therefore required for any mission. Operation at the extremes of the SOA may also heighten the chances of single-event effects (SEE), particularly single-event burnout (SEB).

- The critical drain voltage V_{crit} refers to the drain voltage above which drain and gate leakage currents and/or performance degradations become time dependent. Above V_{crit}, the leakages increase in time with a rate dependent on the drain voltage. Ideally V_{crit} lies beyond the SOA, but in practice, the V_{crit} may be lower than $V_{DSmax.safe}$. Operation with voltages beyond V_{crit} has implications for long-term reliability (see Section 3, Appendix D, and Appendix H).

- Maximum safe drain current $I_{Dmax.safe}$ refers to the maximum safe peak instantaneous current under RF or DC conditions. The drain current at which failures or degradations occur is at least 2× higher.

- A recommended drain quiescent DC voltage Q-point V_Q may optionally also be specified; however, the circuit designer should be responsible for ensuring that all maximum safe ratings are never exceeded during RF operation. This may be done using simulations, load pull data, or measurements. (Note that for Class A amplifiers, the peak drain voltage is approximately $2\times V_Q$; for a class AB amp approximately $3\times V_Q$; for harmonically tuned amps such as Class E, F, F^{-1}, etc., peak drain voltage can be higher yet).

- Maximum safe reverse gate-source voltage $V_{GSmax.safe}$ refers to maximum safe peak instantaneous reverse voltage under RF or DC conditions. The catastrophic gate-source DC burnout voltage shall be 2–3× higher in magnitude.

- Maximum safe forward gate-source current $I_{Gmax.safe}$ refers to maximum safe peak instantaneous forward current under RF or DC conditions.

- A gate SOA refers to the regions in the I_G vs. V_{GS} plane for which no catastrophic damage ensues. Operation at the extremes of the SOA, while not catastrophic, may still incur gradual degradations. Reliability assessments are therefore required for any mission.

- The RF survivability limit refers to the pulsed RF input level (dBm) for which no change in DC characteristics, output power, or small-signal s-parameters occurs. The conditions of this definition are (in the absence of specific requirements):

  - Frequency within its normal operating band
  - Pulse duration 10 μsec
  - Pulse repetition rate 1 kHz
  - Duration of pulse train 1 minute

These conditions should be tailored to reflect the actual mission whenever possible.

In the following sections, the tests necessary to establish these limits to ensure robustness in a long-term mission are described.

2.1 DC Drain Safe Operating Area (SOA) Determination

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
100	3	once	✓	✓	✓	realistic HEMT dimensions

GaN HEMTs are well suited as the output stages in RF/microwave power amplifiers. In order to operate the HEMTs in a reliable way, there are limitations on the maximum voltage, current, and power that must be observed. The RF loadline (or more generally the load figure) must always remain well below the burnout or breakdown threshold of the HEMT. In order to qualify power HEMTs, the safe operating area in the I_D vs. V_{DS} plane must be determined. The purpose of this destructive qualification test is to map out the boundaries of the drain safe operating area (SOA) so that maximum conditions may be established, and to justify any deratings that may be necessary.

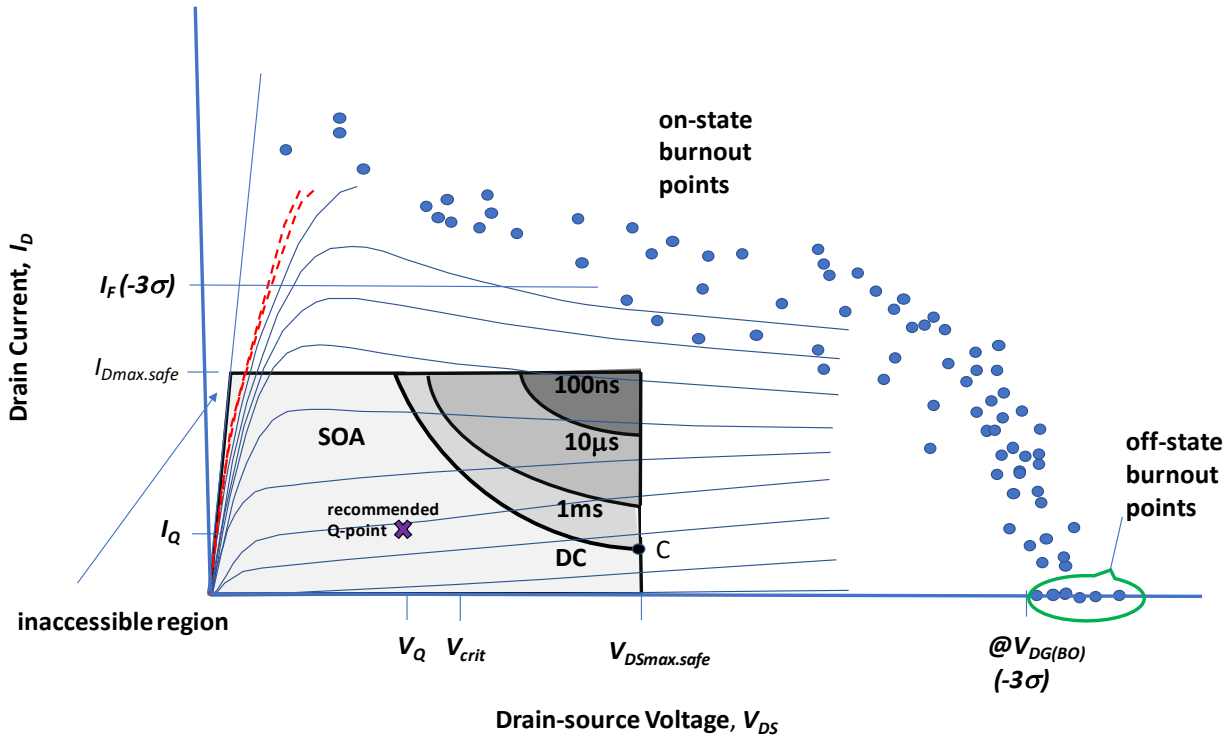


Figure 2-1. Example drain IV plane and common source: characteristics of a GaN HEMT showing the safe operating area (SOA). The dots show the burnout points that must lie outside the drain SOA. The drain SOA becomes larger for short pulses. The critical voltage V_{crit} defines the onset of time dependent degradation. A recommended Q-point is often optionally specified. A critical voltage V_{crit} may exist where gradual time-dependent degradation can occur. Point C shows the recommended stressing condition for power cycling tests (Section 2).

Figure 2-1 shows the DC I_D–V_{DS} plane for a GaN HEMT. The DC common source characteristics of a device are shown in this figure along with recommended maximum safe drain voltage $V_{DSmax.safe}$ and maximum safe drain current $I_{Dmax.safe}$ limits. Also shown are maximum constant power contours for DC and for pulsed operation with pulse repetition rates of 100 Hz with 1 msec, 10 µsec, and 100 nsec pulsewidths. (The 100 Hz / 100 nsec case encompasses the entire IV plane.) In the ideal case, these are hyperbolae for a constant maximum temperature. If thermal resistance is constant, they are ideal. But in actuality the thermal resistance of a GaN HEMT may not be a constant, causing these curves to deviate from ideal hyperbolae. (See Section 3.3 for discussion.)

The test should be conducted by driving the device with a constant gate-source voltage to establish a certain bias condition. The gate voltage steps range from negative values (blue solid curves) to slightly positive values (red dashed curves). Next, the drain voltage should be ramped up or stepped upward with fixed time intervals until failure occurs. Different step durations may also be explored. However, they should be relatively slow compared to the thermal time constant(s) of the die and its mounting. The durations should typically be 100 ms or 1 sec. Each point on the IV plane where a failure occurs is marked (see the dots in Fig. 2-1). By selecting various gate biases, a series of failure points is found, as shown in the figure. The lower left boundary of all these points establishes the safe operating area of the transistor.

The safe operating area so obtained may be a combination of thermal and electrical failures and is considered a DC drain SOA. It may also be desirable to minimize the thermal interactions by pulsing the drain voltage with a short-duration pulse rather than a DC condition, as described in Section 2.1.1 below.

A measurement of the drain current during the DC steps or pulses is recommended. This drain SOA test should be performed with the device at the highest planned elevated baseplate qualification temperature or at a baseplate temperature of 150 °C, whichever is most appropriate. A failure is defined when the drain current suddenly changes. Depending upon the GaN process technology, the failure will manifest itself as either a shorted or high-current mode, or the device becomes an open circuit.

The drain SOA test is statistical in nature. There will be some spread in the characteristic burnout failure points due to device variability. It is important to have a relatively large sample size in order to obtain a conservative drain SOA. It is recommended to have at least 100 devices devoted to this test. It is also recommended that the devices be drawn from at least three wafers or production lots so as to sample the production variability of the drain SOA. Unfortunately, the drain SOA test is a destructive test. On-wafer tests or packaged devices are also suitable.

The geometrical size of the device selected for drain SOA testing should be representative of that to be used in the final application. If a much smaller-area discrete device (with fewer or narrower gate fingers) is used, the drain SOA results tend to be more favorable than with a realistically sized discrete device. In the case of GaN MMICs, the drain SOA test should be performed on a representative MMIC test chip tailored for the purpose and representing a similar topology and circuit design to the actual MMICs to be used.

Under off-state conditions, burnout occurs due to catastrophic breakdown, a purely electrical rather than a thermal event. It is especially important to characterize this regime of operation, which is described in Section 2.2 below. Under on-state conditions, at low voltage, the burnout tends to occur at a high-current condition. It may be necessary to actually apply a forward voltage on the gate in order to achieve burnout at low drain voltages. This possibility is indicated by the low-voltage IV curves shown in red in Fig. 2. A certain region of the IV plane is inaccessible due to series resistance in the intrinsic device itself or in the source or drain contacts.

Figure 2-1 shows the maximum safe drain-source voltage $V_{DSmax.safe}$ as the rightmost boundary of the drain SOA. Several considerations enter into the establishment of $V_{DSmax.safe}$. Its value should be at least 2× or 3× less than the catastrophic breakdown points shown by the dots. See Appendix D for more rationale for this recommendation. $V_{DSmax.safe}$ also is tied to a reliability metric. It is recommended that the $V_{DSmax.safe}$ rating be set such that operation up to $V_{DSmax.safe}$ guarantees a certain reliability. It is believed that GaN HEMT reliability has a dependence on not only the channel temperature but also the electric field or drain voltage in many devices. In fact it has been suggested that a TDDB-like (time-dependent dielectric breakdown) occurs in GaN HEMTs above a certain critical voltage V_{crit}. See Section 3 for details. Methods to model the voltage dependence of the reliability on the drain voltage V_{DS} are proposed, and a means to determine the required $V_{DSmax.safe}$ to assure a required reliability is provided in Appendix H.

Another limit on $V_{DSmax.safe}$ comes from the need to survive cosmic rays in a space environment. The single-event phenomena in GaN HEMTs are discussed in Section 7. A further derating of the $V_{DSmax.safe}$ rating may be necessary in order to preclude single-event effects such as catastrophic failure. The $V_{DSmax.safe}$ rating is therefore constrained by multiple factors—derating for burnout, reliability, and immunity from single-event effects.

2.1.1 Pulsed-Drain Safe Operating Area (SOA) Determination

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
100	3	once	✓	✓	✓	realistic HEMT dimensions

In similar fashion, it is also possible also to generate a pulsed SOA in the $I_D - V_{DS}$ plane. The resulting pulsed-drain SOA is represented in Fig. 2-1 by the shaded regions for two different example pulsewidths of 10 µsec and 100 nsec. The methodology is like the DC case except that the drain voltage V_{DS} is pulsed at successively higher values for the desired duration in single-shot fashion with constant gate bias. The pulse length is chosen to be short, compared to the thermal time response of the DUTs. This is done because short pulsewidths may better represent the usage conditions of a particular mission. As with the DC SOA testing, the pulse height is made successively higher until a catastrophic failure is reached so that the SOA reflects an electrical burnout or breakdown effect with less thermal interaction. Although the instantaneous power dissipation can be large, the thermal rise may be quite small for sufficiently short pulses. For very short pulses, the SOA becomes essentially a rectangle bounded by maximum voltage and current limits, with essentially no thermal component. The temperature rise in such case is adiabatic, meaning that heat does not diffuse significantly from the channel region in the short pulse time.

It is recommended that the pulsed testing be performed at a repetition rate that is similar to that used in the mission, so that the average temperature of the channel is realistic. For general characterization, it is recommended that the pulsed-drain SOA be determined at a baseplate temperature of 250 °C with a 1 msec single-shot drain voltage pulse duration (in the absence of specific requirements). The baseplate temperature of 250 °C is intended to replicate a condition where a device in normal operation has a high channel temperature by virtue of its dissipated power. In these pulsed SOA tests, there is essentially no dissipated power, therefore it is necessary to elevate the baseplate temperature to mimic usage conditions.

2.2 DC Off-State Burnout

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
50	3	once	✓	✓	✓	realistic HEMT dimensions

Since a power device is often required to stand off a relatively high voltage, a special subset of tests should be devoted to off-state breakdown. The procedure would be like the drain SOA test described above; however, the device remains in the off state with the DC gate voltage in hard pinchoff. To include breakdown due to buffer layer or substrate leakage, the drain voltage should be ramped or stepped with reverse-gate bias set to the maximum safe rated reverse gate voltage $V_{GSmax.safe}$ as determined in Section 2.3 (nonoperational test) and described further in Appendix D. In Figure 2-1, the off-state burnout points are shown explicitly.

It is recommended that the off-state burnout testing be performed with DC ramps or steps. The step durations should be 100 msec or 1 sec in duration. Although there is essentially no thermal dissipation to consider with the device in the off state, the channel temperature may always be higher than the baseplate under usage conditions. This happens when the device is switched off immediately after an RF pulse, for example, and the channel temperature has not yet cooled to baseplate. If the breakdown is driven by buffer layer leakage, then failure would be sensitive to the device channel temperature. It is recommended

that this test be performed at the maximum anticipated channel temperature in usage or at a baseplate temperature of 150 °C, whichever is most appropriate. The quantity of devices subjected to this test should be approximately 50, and should be drawn from at least three wafers or production lots.

2.3 DC Gate Damage Threshold

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
48	3	once	✓	✓	✓	• realistic HEMT dimensions • 24 DUTs forward, 24 reverse polarity • both operational and nonoperational states

Under some nonoperating or operating conditions, the gate terminal of a discrete HEMT or the input terminal of a GaN MMIC may be exposed to a high DC or RF power. The purpose of this test is to quantify the damage threshold for the gate electrode for DC electrical stress (Christiansen, 2012). The order of applied biases must also be considered to avoid part damage or heating. For example, the source should be grounded and a gate bias more negative than the threshold voltage, V_{th} applied prior to applying the drain bias. This sequence of applied bias minimizes the risk of open-channel conduction and overheating, oscillations, or damage.

For a discrete HEMT, the gate terminal voltage is stepped until a sudden and permanent change in the drain current I_D, gate current I_G, "on"-resistance R_{Don}, or other parameters of interest is observed. This requires alternating the gate stress with intervening measurements at typical bias conditions. For a MMIC, the RF input terminal voltage or the DC gate-biasing terminal (as appropriate) is stepped, again with intervening measurements of DC parameters. For a MMIC with multiple stages, it would be useful to separately find the gate SOA for each stage if the stages have independent biasing terminals.

It is recommended that the durations of the steps should be relatively slow compared to the thermal time constant(s) of the die and its mounting—typical step times are 100 ms or 1 sec. Both polarities of the gate voltage or terminal voltage shall be used. One set of samples should be devoted to the forward Schottky gate polarity and another set for the reverse polarity. The tests are intended to be destructive to the transistors and to find both the reverse DC gate voltage and the forward DC gate current that cause immediate damage. The tests should be conducted at the maximum channel temperature anticipated in usage, or at a baseplate temperature of 250 °C whichever is appropriate. The drain voltage should be in the range 25%–50% of the rated drain voltage for operational tests. The drain and source should be shorted for nonoperational tests.

An example of a nonoperational gate DC SOA is illustrated in Figure 2-2. A typical IV characteristic with source and drain shorted is shown in the figure along with the points at which changes in the drain current I_{DSS} (drain current with $V_G = 0$ V at 50% of max rated safe drain voltage) were noted. In the forward direction, the gate IV characteristic was unchanged, but I_{DSS} was affected. In the reverse direction, a sudden breakdown or catastrophic event is noted at the points shown. Based upon these results, the gate DC SOA corners are placed at (I_G, V_G) values of (+150 mA/mm, +2 V) in the forward direction and (–20 mA/mm, –10 V) in the reverse direction.

It is recommended that the sample sizes be as follows:

Condition	V_{DS}	
Nonoperational, reverse-gate bias	0 V	12 samples
Nonoperational, forward-gate bias	0 V	12 samples
Operational, reverse-gate bias	25–50% of $V_{DSmax.safe}$	12 samples
Operational, forward-gate bias	1–10% of $V_{DSmax.safex}$	12 samples

Note that the operational forward bias gate burnout test poses some special difficulties. It is possible that application of sufficient gate forward bias while the drain voltage remains at 1–10% of $V_{DSmax.safe}$ could cause drain current to exceed the drain SOA. In cases such as this, current should be limited to $I_{Dmax.safe}$ or a realistic drain circuit impedance or load shall be employed for the test.

For GaN HEMTs, the damage threshold currents should be reported in normalized units of current per unit gate width (for example, milliamps/mm). For GaN MMICs, the threshold currents should be reported as a current (for example, milliamps).

For GaN MMICs the same procedure should be used where the DC gate bias input terminal is driven with a similar step voltage, with the drain or power supply terminal at its nominal value for operational tests. For nonoperational tests, all other terminals are grounded, simulating a worst-case unpowered state.

The device size selected for gate damage threshold testing should be representative of that to be used in the final application. If a much smaller area discrete device (with fewer and or narrower gate fingers) is used, the gate destruction levels tend to be more favorable than with a realistically sized discrete device. In the case of GaN MMICs, this gate current test should be performed on a representative MMIC test chip tailored for the purpose and one that represents a similar topology and circuit design to the actual MMICs to be used.

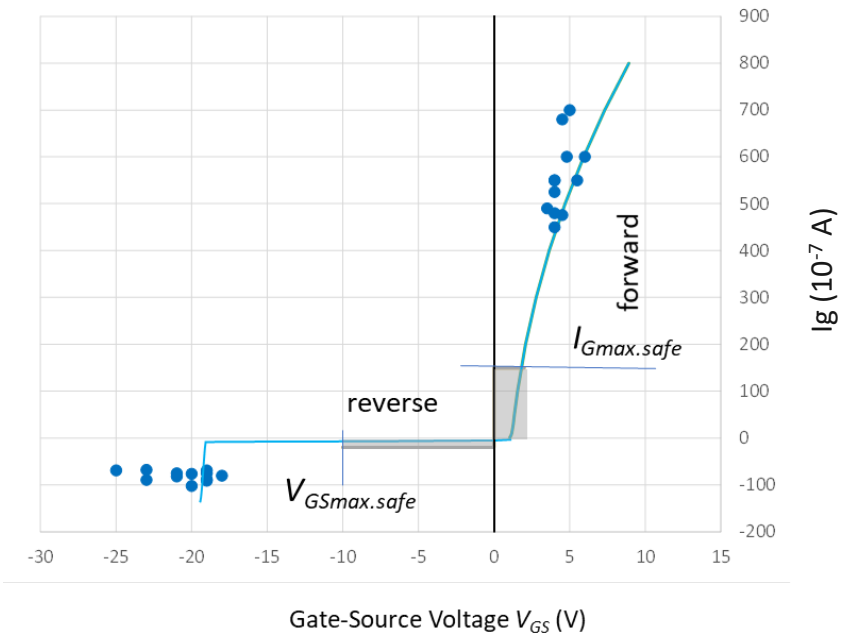


Figure 2-2. Example gate IV plane of a GaN HEMT showing the maximum safe gate voltage and current. These points are in the nonoperational mode (V_{DS} = 0). The dots show the burnout points that must lie well outside the gate safe operating area (SOA).

2.4 Off-State High-Voltage Screen

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
100%	100%	100%	✓	✓	✓	100% test on all devices from each wafer, 2% fail criterion

The HEMTs or MMICs should be 100% screened in the off-state at rated maximum safe drain voltage $V_{DSmax.safe}$ and maximum rated safe reverse gate voltage $V_{GSmax.safe}$ in air at an ambient temperature at least as high as the anticipated usage temperature, or at 150 °C for a minimum of 1 second. This test should be performed on a wafer-by-wafer basis: the "population" is defined as all the devices from a given wafer. Any device that breaks down or has a drain or gate leakage current after this exposure that is greater than the specified values should be removed from the population. Also, the drain or gate leakage at the elevated test temperature shall not increase by more than 50% as a result of performing this test. This qualification will consist of demonstrating that no more than 2% of product fail these requirements. It also consists in developing the leakage current to be used in this screen for future product. Any wafer containing devices or product failing these requirements shall not be used for subsequent reliability or qualification testing or spaceflight.

In addition to a screen for defects, the off-state voltage condition may also serve as a monitor for the far right side of the SOA characteristic and for monitoring the $V_{DSmax.safe}$. If the gate current does not exceed a certain value, this may correlate well with and have a catastrophic breakdown voltage in exceedance of 2× – 3× $V_{DSmax.safe}$. This correlation must be verified in advance. It may be an efficient way to monitor for a weak wafer or lot. The specification for the leakage current depends upon the correlation obtained to catastrophic breakdown, but a criterion on the order of 0.1–1 mA/mm may be reasonable. However, it

should not be used as a substitute for the full determination of the SOA as described in Sections 2.1 and 2.2.

The off-state screening test recommended here is not intended to mimic HTRB (high-temperature reverse-bias) tests that are industry standard in Si technologies. There, the HTRB test is often performed on a sample basis as part of lot acceptance, often at 125 °C for 1,000 hours. The results are graded on a pass/fail basis against a leakage current specification or increase of leakage current. In the GaN testing recommended here, a similar qualification test for off-state intrinsic reliability is recommended below in the Q4 DC bias conditions (see para. 3.1) as an accelerated test.

This off-state high-voltage screen recommended here is for a much shorter time—1 second. It resembles the "DWV" (dielectric withstanding voltage) test performed on 100% of ceramic capacitors at an elevated voltage to screen out defects. If a processed GaN wafer has a high defect density (whether from its starting material or the many processing steps), the goal of this test is to remove that wafer from further qualification tests. There is nothing worse than performing qualification lifetests only to find early failures or out-of-family results. When this happens, the qualification is at best questionable and at worst invalidated. The purpose here is to remove potentially defective wafers from qualification. Further, it is important to remove potentially defective wafers from consideration for spaceflight for the same reason.

2.5 ESD

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
60	3	once	✓	✓	✓	• 40 DUTs HBM • 20 DUTs CDM

The GaN transistors or MMICs should be subjected to ESD (electrostatic discharge) testing. It is recommended that the human body model (HBM) and the charged device model (CDM) be used for ESD testing. It is recommended that the so-called machine model (MM) not be adopted for ESD tests. The tests should be conducted at room temperature (or a selected measurement temperature) using a test fixture tailored to the package or configuration of the HEMT or MMIC. The ESD threshold category levels for HBM and CDM are determined using this test.

In many cases, dry nitrogen gas is used for purging space hardware while in storage or in various stages of integration before launch. It should be pointed out that the dry nitrogen environment can increase the risk of ESD problems. It is important to treat any assembled hardware containing GaN HEMTs or MMICs as ESD-sensitivity class 0. Some GaN devices in the off-state subjected to ESD pulses of sufficient magnitude can be destroyed catastrophically with TLP (transmission line pulser) waveforms with durations of only approximately 100 ns (Tazzoli, 2007). The mode of failure is that a filament is formed between the electrodes, typically between drain and source. The filament forms because of the negative differential conductivity of the semiconductor material at high electric fields. When a pulse is applied between gate and source, degradation of the Schottky barrier occurs with reverse-gate polarity ESD pulses of ~30 V. It is important to handle these devices correctly during space hardware assembly and integration at all stages.

The HBM tests should be performed in accordance with MIL-STD-883K Method 3015.9 (2015). The CDM tests should be performed in accordance with JEDEC standard JESD-22-C101F (2013).

For HEMTs the ESD tests should be performed under several different configurations:

- HBM pulsed drain with gate floating, both polarities
- HBM pulsed drain with gate grounded, both polarities
- HBM pulsed gate with drain floating, both polarities
- HBM pulsed gate with drain grounded, both polarities
- CDM on gate with source and drain grounded, both polarities
- CDM on drain with gate and source grounded, both polarities

The standards call out the number of DUTs (typically 5 per configuration), the number of pulses per level (typically 10 pulses per level), and the numbers of levels. Since there are a total of six configurations listed above, each having two polarities, a total of 60 DUTs is required—40 for the HBM and 20 for the CDM. Samples should be drawn from at least three lots or wafers.

For MMICs, the HBM should be applied to each possible pair of terminals in succession, in accordance with the standards mentioned above. For MMICs, the CDM should be applied to each individual terminal in succession with the other terminals grounded. The MMIC DUT quantities needed to satisfy the standards depend upon the number of MMIC pins. Samples should be drawn from at least three lots or wafers.

The failure criterion should be that the gate and drain leakage currents exceed the room temperature specification values or exhibit an increase of 50%. In many cases full destruction might occur prior to this failure criterion.

2.6 RF Burnout/Survivability

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
12	3	once	✓	✓	✓	realistic HEMT dimensions

Despite the desire to operate GaN HEMTs or MMICs under conservative de-rated conditions, there are situations where the device could be exposed to a damaging RF pulse condition. The purpose of this requirement is to establish the threshold or condition for damage under unexpectedly high RF drive. In certain applications, knowledge of this level is necessary to qualify the device. A destructive RF burnout test is required in these cases (Chen, 2007). Certain GaN-based LNAs have shown remarkable robustness to RF input overdrive with included Schottky field plates, and high-impedance gate-bias circuits (Colangeli, 2013).

It is recommended that the HEMT or MMIC be operated during RF burnout tests at its maximum drain voltage with an operating point at a relatively low current of 20% of maximum current. Then its input should be subjected to an in-band pulsed RF input condition. In the absence of specific mission requirements, the following recommendations should be followed. For GaN HEMTs, the input and output should be matched to achieve an optimum PAE. For GaN MMIC power amplifiers, the source impedance should be 50 Ω and the output matched for an optimum PAE. The following pulse train characteristics are recommended:

Frequency	centered within its normal operating band
Pulse duration	10 μsec
Pulse repetition rate	1 kHz

Temperature	25 °C
Input level	stepped in 1 dB increments starting from 5 dB below the 1 dB compression point until destruction
Duration of pulse train	1 minute

Before and after each 1-minute exposure, the device should be measured to determine its small-signal gain, output power, and DC parameters changes (R_{Don}, V_{th}, I_G, and I_D). The point at which the small-signal gain or output power changes should be recorded. A failure criterion for the small-signal gain or output power change should be ±1 dB or out-of-specification changes in the DC parameters. A sample size of 12 devices is recommended—four devices from each of three lots. The recommended test temperature is the maximum anticipated temperature of the mission baseplate, or room temperature. The DUTs require RF fixtures or RF packaging, although at lower frequencies, wafers could be tested using an RF probe station.

2.7 Temperature Cycling

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
75	3	once	✓	✓	✓	mission-like packaging

In many applications, the HEMT or MMIC will be cycled on and off many times during the mission and the ambient or baseplate temperature concomitantly cycled. In other applications, the temperature of the ambient or baseplate varies over a wide range irrespective of whether the device is powered. For this reason, an explicit temperature cycling test to assure the robustness of the device should be considered. GaN RF power devices tend to be relatively large in area, and shear stresses can be concomitantly large. It is important to test the actual die size(s) that are intended for usage for a realistic qualification. The purpose is to test the die or the die and its immediate surroundings as packaged. The failure mechanisms of interest here are the delamination or cracking of the die, its passivation of various interconnect layers, the airbridge integrity, the bonding pad delamination, or gate metal lifting. The die should be bonded or soldered to the substrate as it might be in the final application. However, the bondwires or the package need not be identical to the final configuration since the purpose of this test is to ascertain the temperature cycling robustness of the die and die layers alone, not the bondwires, solder, and other components of the packaging. The device need not be powered during the temperature cycling.

The test method for temperature cycling as defined in JEDEC standard JESD22-A104D (2009) is recommended except that the temperature extremes should be from –60 °C to +200 °C. The standard provides appropriate temperature ramp and dwell times for the acceleration of the mechanical creep related failure mechanism. This wider temperature range is recommended owing to the higher temperature extremes anticipated by the GaN technology. A typical mission might require 100,000 cycles of the die temperature (not junction temperature) from 65 °C to 150 °C. Another JEDEC recommendation (JEDEC JESD47-I.01, Annex A, 2016) shows how to estimate the number of test cycles needed. The simple Coffin-Manson model is used here for lack of a defensible, more comprehensive model for a GaN chip. The materials of interest here are metals, dielectrics, and semiconductors (not solder), and for these, a conservative Coffin-Manson exponent $q = 4$ is typically used. A typical example mission consisting of 100,000 cycles, is translatable to

	Temperature cycling
Example Mission	Qualification Test
T_{min} = 65 °C	T_{min} = –55 °C
T_{max} = 150 °C	T_{max} = 200 °C

ΔT = 85 °C	ΔT = 255 °C
N = 100,000 cycles	N = 1,250 cycles

Therefore, it is recommended that a temperature cycling test be performed with these conditions. If mission requirements differ, the same approach may be applied to arrive at the qual test conditions. It is recommended that 3 lots with 25 samples per lot be utilized as recommended by JESD47-I, Tables 2 or 3. Before and after all the cycles, the device parameters of Sections 3.5 and 3.6 of this document should be measured with failure criteria as in Section 3.7. Bias, temperature, frequencies, and other measurement conditions shall be identical before and after the cycles. There should be zero failures. It is also recommended that one or more uncycled DUTs be maintained as test controls.

2.8 Power Cycling

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
36	3	once	✓	✓	✓	mission-like packaging

In certain missions, the quiescent bias is not applied continuously but rather is cycled on/off for various durations. This is distinct from a pulsed RF waveform but is rather the situation where the power supply itself is switched on/off. Because the GaN HEMT layers are piezoelectrically active, this cycling of bias causes mechanical strain to be applied for a while, then removed. The application of mechanical strain to a piezoelectric structure such as a GaN HEMT has well-known electrical effects (Chang, 2009) and can also generate traps and dislocations (del Alamo, 2008; Marcon, 2013). The issue addressed by this power cycling test is whether cyclic voltage/temperature/power variations that may occur in a space mission have additional effects. Therefore, it is recommended that when appropriate for a particular mission, a test be carried out by cycling the power. It is also recommended that the value of V_{crit} first be determined (see Section 3.4). It is strongly recommended that the power cycling test be performed at a voltage greater than V_{crit} if allowed by the DC drain SOA.

It is recommended to power cycle devices from 3 lots, 12 devices from each lot. Lot-to-lot variation in the AlGaN/GaN built in strain may be an important contributor to the cycling behavior. Therefore, three lots should be selected from different batches of starting wafer material. They should be packaged in a mission-like fashion.

A recommended test procedure is to operate the DUT at a quiescent DC stress condition selected at the upper right corner of the drain DC SOA (see point “C” in Fig. 2-1), which is above the V_{crit} value. The baseplate temperature should be like that in the mission or at 150 °C if there are no specific requirements. The temperature cycles so incurred are different from those of Section 2.7 because here the temperature cycles are internal in nature, arising from internal power dissipation rather than externally supplied. The stress gradients introduced by the temperature coefficients of expansion mismatches of all the layers is very different than when temperature is externally cycled. It is recommended to operate for 1 minute at the Fig. 2-1 on-state bias SOA Point C, then 1 minute with power removed from all terminals (a total 2-minute period with 50% duty cycle). Without specific mission requirements, it is recommended that the DUT be operated in this manner (1 min. on / 1 min. off) for a duration of 168 hours (1 week), giving a total of approximately 5,000 on/off cycles. Before and after all the cycles, the device parameters of para. 3.5 and 3.6 of this document should be measured with failure criteria as in para. 3.7. Bias, temperature, frequencies, and other measurement conditions shall be identical before and after the cycles. There should be zero failures. It is recommended to also maintain one or more uncycled DUTs as test controls.

3. HEMT Reliability Tests for Intrinsic Failure Modes

In this section, the longer-term reliability tests that are required are described for both HEMTs and MMICs. The HEMTs embedded within the MMICs are the active device addressed in this series of testing. There are certain intrinsic or wear-out types of failure modes that are unique to GaN HEMTs that are of interest. Other GaN MMIC and device structure and fabrication reliability concerns include the ohmic contacts, Schottky gate, substrate via holes, airbridges, MIMCAPS, resistors, and interconnects. The following three main stressors are available for accelerated testing for reliability:

- High temperature: potential for SiN-AlGaN interface degradation, diffusion, and trap formation; potential for ohmic contact degradation; potential for gate metal migration

- High electric fields: field-assisted electron tunneling into traps, piezoelectric effect strain damage, "quasi" time-dependent-dielectric and/or barrier breakdown, electrochemical reactions, etc.

- High currents: electromigration, resistor burnout, impact ionization

Despite all the failure mechanisms listed in Section 1.1, there are only three stressors for reliability testing. Many of these mechanisms are unique to GaN HEMTs. Therefore, with only three main stressors available, it is likely that any one type of stress will trigger multiple failure mechanisms. With this in mind, tests for intrinsic GaN HEMT reliability must be designed carefully.

3.1 GaN HEMT Operation and Multiple Failure Modes

In the previous generation of GaAs devices (originally mostly dedicated to producing LNAs), DC-accelerated testing at multiple temperatures became the norm. This was an effective strategy for reliability testing since these devices operate usually under small signal conditions for which DC stress is a reasonable approximation. Further, there was only one dominant failure mechanism in the early generations of GaAs devices and MMICs. This failure mechanism was "gate sinking," where the gate metal interdiffuses with the semiconductor and produces predictable and well-understood changes in characteristics. For gate sinking, the changes in I_{DSS} are closely correlated to the changes in the s_{21} magnitude. This serendipitous state of affairs enables DC-accelerated testing to determine the Arrhenius relationship (activation energy and time-scale coefficient) for reliability predictions. Typically, tests are done at three temperatures, to determine median lifetimes or failure probabilities. In fact, a JEDEC specification JEP118A was developed to recommend the procedures for GaAs HEMT testing and analysis. Unfortunately, with GaN devices, the situation is not as straightforward. For GaN devices, traditional three-temperature testing at a single DC operating point is not sufficient. This is because there is no single DC test condition that can be used to accelerate the various known failure mechanisms. Instead we recommend a broad brush or brute force approach where many parameters and measurements are made in the quest to identify failure modes, especially those hidden or not operating under the typical or standard lifetest conditions.

Many manufacturers have provided three temperature DC lifetests in which a ΔI_D failure criterion is used for GaN transistors. (Note that a DC measurement of I_{DSS}—the drain-source current measured with gate shorted to source—is often not feasible for GaN power devices as it is destructively large. Instead, the drain current change ΔI_D with a fixed, predetermined negative gate voltage is often substituted.) Unfortunately, the correlation to changes in s_{21} have not been established in all cases. In GaN HEMTs the presence of much higher electric fields and higher current densities suggests that there may be other stressors beyond thermal acceleration. Extrapolations to usage temperatures based only on DC stress and DC measurements may not necessarily predict the long-term reliability under actual RF usage conditions.

There have been a few attempts (Chini, 2012; Paine, 2015a-c; Coutu, 2016) to address the issue of competing multiple failure mechanisms in GaN HEMTs. The multiple mechanisms are a function of the materials (such as the epitaxial layers, passivation, metals, etc.), the processing (the ohmic contact formation, the gate stack and lithography, etc.), and the device design (such as a field plate design, T-gate, the source-drain recess spacing, etc.). The exact mixture of failure modes that might be experienced under actual spaceflight usage conditions also depends for a given device upon the particular RF/microwave loadline (more correctly the load figure) and/or the matching and loading impedances. Figure 3-1 shows IV curves from DC and pulsed IV measurements for a typical microwave power HEMT. Pulsed IV (PIV) test equipment is now readily available from several companies (Tsironis, 2009).

In order to assess the multiplicity of failure modes that might affect long-term reliability in a GaN power amplifier application, the RF loadline (or more properly the "load figure") should be considered. In Figure 3-1 is shown a family of DC IV characteristics of a typical RF HEMT (solid red lines), along with the corresponding pulsed IV characteristics (squares). A large discrepancy between static versus pulsed IV curves exists because of the aforementioned trapping phenomena. Also shown are some typical loadlines for an RF amplifier. The first is an ideal or resistive Class A loadline. In practice, a loadline is actually not purely resistive since especially at high frequencies, the reactance and parasitics become important. For this reason, under a more realistic Class A operation, the loadline becomes elliptical, as shown. Also shown for comparison is a Class F^{-1} (inverse Class F) load figure, which is considerably more complex. The Class F^{-1} amplifier approach is one of many that improves narrowband efficiency by controlling the harmonics—in this case tuning the impedance at the odd harmonics to be a short circuit and the even harmonics to be an open circuit—thus dissipating zero harmonic power. The Class F^{-1} load figure passes through very different regions of the IV plane than the Class A load figure does. Therefore, if there are different failure mechanisms extant at different operating points in the IV plane, this load figure would be expected to produce different reliability results. This in fact has been observed for certain GaN devices.

In the following sections, recommendations are made concerning reliability testing of GaN HEMT devices and MMICs. Since the most common application of GaN HEMTs is for the generation of RF or microwave power, then it would seem that RF-driven accelerated lifetesting would be the most efficacious test methodology. However, there are many practical problems with this approach. A particular HEMT device or MMIC process might be used in various applications covering a wide variety of frequency bands, different power levels, different levels of saturation, or diverse pulse or modulation schemes, and having different loadlines or load figures. Depending upon the exact RF loadline for a particular design, a different set of failure modes might be important, sometimes competing with each other. It would be impossible to cover all these possibilities. Not to mention the expense of performing multitemperature, multicondition lifetests in a properly fixtured RF/microwave test set. RF-driven stress lifetest sets with accommodations for statistically significant device quantities under different stressing conditions are expensive and require very high levels of engineering expertise. Instead, it is proposed here that much reliability information can be gleaned by performing DC-only lifetests, by extension to the methods of the JEDEC standard JEP-118A.

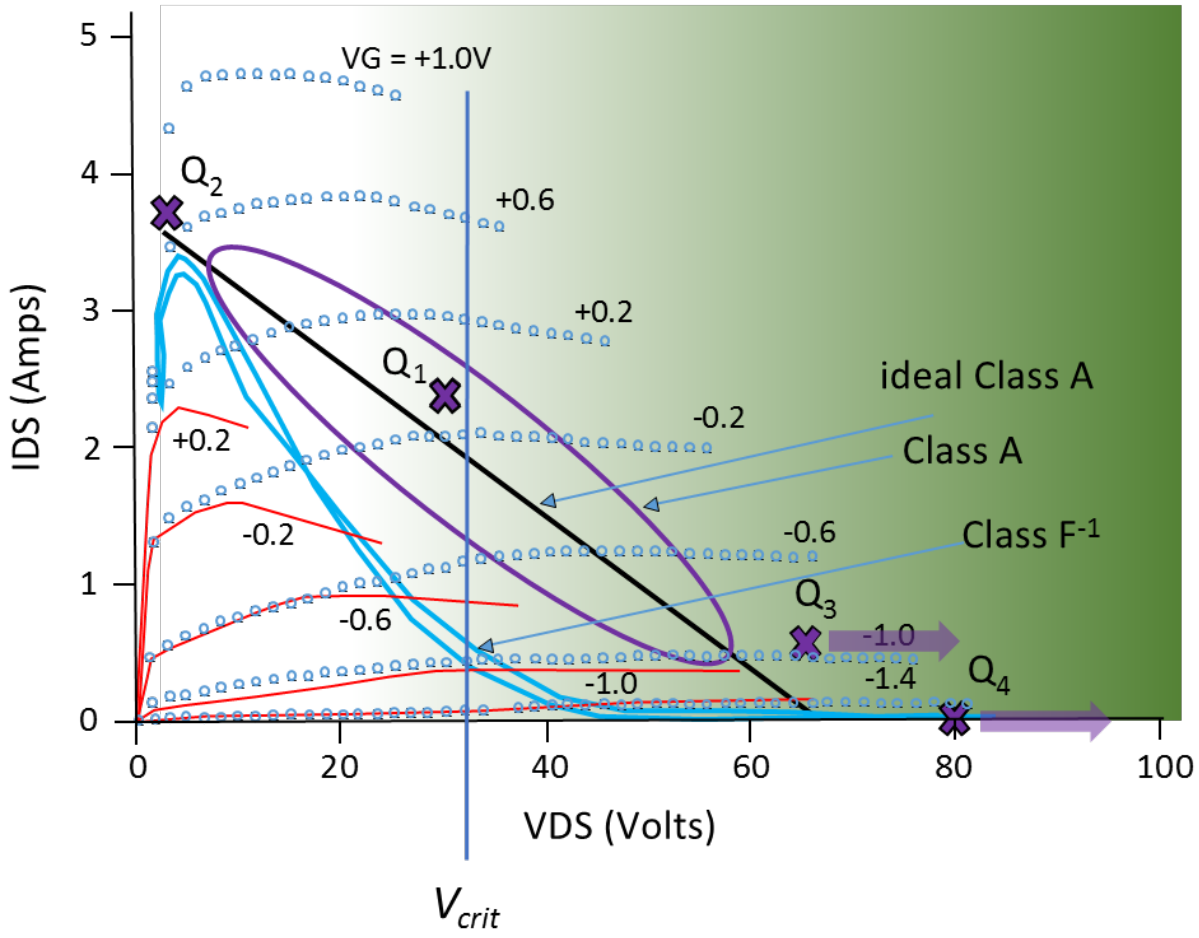


Figure 3-1. DC (lines) and pulsed IV (points) characteristics of an RF power GaN HEMT, and representative loadlines, with four proposed operating Q-points for DC reliability testing. The shaded region below V_{crit} may exhibit quite different electric field-driven failure modes than the region above it does.

Since GaN HEMTs may have different failure modes (or different mixtures of failure modes) depending upon the RF loadline (or load figure), it seems reasonable to decompose any conceivable RF loadline into regimes where different failure modes might exist. In Fig. 3-1 four possible DC Q-points (quiescent points) that are believed to stimulate different failure mechanisms are identified:

- Point Q1 is a high-power operating point. It is similar to one traditionally chosen for DC three-temperature lifetests. It is near the center of the IV plane, provides a maximum temperature rise through self-heating, and provides high thermal acceleration. It also provides the maximum thermal gradient(s) in a HEMT. This is the approach usually taken for GaAs lifetesting as recommended in JEP118A. Its voltage lies below V_{crit}, should it exist. Properties of Q1 are:

  - It maximizes the thermal stress and the thermal gradients.
  - It stays below the critical voltage V_{crit}.
  - It has been a traditional operating regime for DC lifetesting of GaAs HEMTS; it is not necessarily appropriate alone for GaN.
  - It activates high-temperature failure modes such as gate sinking, buffer layer degradation, 2DEG degradation, contact degradation, Schottky barrier changes, and others.
  - It activates the "missing gate metal" failure mode should it exist.

- Point Q2 is a high-current, low-voltage operating point, also below V_{crit}. At this Q-point, current-driven failure modes such as ohmic contact degradation are accentuated. Properties of Q2 are:

  - It maximizes the current in the source/drain contacts.
  - It has high-current density failure modes, including contact metal migration or hillock formation.
  - It may increase access resistance and cause changes in R_{Don}.

- Point Q3 is a high-voltage, low-current operating point, sometimes referred to as "semi-on." It lies above V_{crit}. At Q3, hot electrons are emphasized since currents sufficient to induce impact ionization may exist in the presence of high electric field. Properties of Q3 are:

  - This operating point maximizes hot carrier generation.
  - Piezoelectric strain is induced.
  - It lies above V_{crit}.
  - It leads to temporary or permanent parameter changes or drifts.

- Point Q4 is a high-voltage, pinched-off operating point with essentially zero drain current well above V_{crit}. Here leakage currents from the gate or drain-source leakage are maximized that could lead to trap generation and device degradation. Properties of Q4 are:

  - It maximizes the piezoelectric strain introduced in the drain-gate region.
  - It lies well above V_{crit}.
  - It leads to surface pitting (especially in the presence of moisture in ambient air) and drain current degradation.

Note that points Q1 and Q2 lie below the critical voltage, whereas Q3 and Q4 lie above it. Depending upon the RF loadline of the HEMT circuit, one or a combination of these mechanisms may dominate the reliability.

It is proposed here that an effective GaN HEMT reliability test campaign can be conducted by operating mainly DC-only mode under test conditions based upon these four quiescent points. Many of the recommendations of JEDEC standard JEP-118A may then be embraced in the DC testing of GaN HEMTs, with certain extensions. It is also proposed that augmentation of the DC-only testing with judicious inclusion of more modest levels of RF testing would complete the reliability picture of GaN HEMT devices. First, however, a brief discussion of possible reliability models is beneficial.

3.2 GaN HEMT Intrinsic Reliability Models

Consider now the standard multi-temperature lifetest as defined in JEDEC JEP-118A. Multiple thermal failure accelerations are prescribed under DC conditions at a quiescent bias point centrally located in the IV plane, such as the quiescent point Q1 as shown in Fig. 3-1. However, since the load figures in Fig. 3-1 traverse such a wide range of currents and voltages, failure modes and reliability may vary widely. Adding to the complexity, there may be a certain drain voltage—the critical voltage V_{crit}—above which the failure modes begin to become influenced by the applied voltage rather than solely the temperature. The critical voltage may be a dividing line between distinctly different failure modes, with a greater contribution due to voltage (or electric field) rather than temperature. In fact, as the drain voltage V_{DS} exceeds V_{crit} by larger and larger margins, failures may be accelerated more and more. Some attention then must be paid to the voltage dependence existing at Q3 and Q4 and the possibility of performing accelerated testing over a range of elevated voltages, shown in Fig. 3-1 by the purple arrows.

Therefore, in the spirit of JEDEC standard JEP-118A, it is recommended that an appropriate time-to-failure model for GaN HEMT devices be considered, different in many respects from one for GaAs HEMTs or HBTs. For voltages below the critical voltage, or when no voltage dependence exists, an appropriate time-to-fail model (t_{50} denoting the median or 50th percentile of failure times) is

$$t_{50} = A\exp\left(\frac{E_A}{kT}\right), \qquad \text{for } V_{DS} \le V_{crit} \quad \text{V-indep} \tag{3-1}$$

which is the usual Arrhenius relationship, expressing accelerated failure times with increasing temperature. However, for voltages higher than V_{crit}, the failure time may also be a function of the drain voltage. Above V_{crit} the reliability model becomes "mixed"—the reliability being determined by both temperature and voltage. The exact form of the model is open to debate at this time. However, three proposed models are provided here that are believed to cover the gamut of the possibilities. The first is a basic model of the form

$$t_{50} = A\left(\frac{V_{DS}}{V_{crit}}\right)^{-n}\exp\left(\frac{E_A}{kT}\right) \qquad \text{for } V_{DS} > V_{crit}. \quad \text{V power} \tag{3-2}$$

Here, the time to fail has an additional multiplier expressing the voltage raised a negative power (power law). This foreshortens the time to fail as the drain voltage V_{DS} increases. Depending upon the fitted value of the power n, the voltage effect is magnified. A second model approach with a stronger voltage effect is

$$t_{50} = A\exp\left(\frac{E_A}{kT} + B\left[1-\left(\frac{V_{DS}}{V_{crit}}\right)^{n}\right]\right) \qquad \text{for } V_{DS} > V_{crit} \quad \text{V- exp} \tag{3-3}$$

where the voltage in excess of the critical voltage now appears in the exponential. This has a more powerful voltage effect, depending upon the fitting parameters. Thirdly, a yet different and more complex approach is to suggest a coupling or interaction between the temperature and voltage drivers, as shown in

$$t_{50} = A\exp\left(\frac{E_A - D\left[V_{DS} - V_{crit}\right]^{m}}{kT}\right) \qquad \text{for } V_{DS} > V_{crit}. \quad \text{coupled V-exp} \tag{3-4}$$

Here the magnitude of the voltage effect is in turn amplified by the temperature, creating a more complex type of interaction. Other similar models are possible.

In these proposed time-to-fail models, the failure time t_{50} is intended to denote the median time to failure, the time by which 50% of the population has failed. The various measured and fitting parameters and their units are the scaling constant A [hours], thermal activation energy E_A [eV], critical voltage V_{crit} [volts], voltage power coefficients m and n [both dimensionless], voltage scaling coefficient B [dimensionless], and voltage-temperature interaction coefficient D [eV/volts^m]. T is the absolute temperature [Kelvins] and k is Boltzmann's constant 8.815×10^{-5} eV/K. Of course, it is true that the more complex the reliability model is, the more measurements are required to determine the coefficients. Figure 3-2 plots the voltage dependence of the median times to failure t_{50} for the four models. The following collection of coefficients and conditions were selected:

T_{ch} = 200 °C	mission channel temperature
E_A = 1.4 eV	thermal activation energy
V_{crit} = 25 V	critical voltage
m = 0.4	voltage power coefficient
n = 3	voltage power coefficient
$A = 1.5 \times 10^{-8}$ hours	failure time scaling constant
B = 0.2	voltage scaling coefficient
D = 0.025 eV/volts^m	voltage-temperature interaction coefficient

The models can take on many different shapes, depending upon the fitting parameters. The V-indep model has no voltage dependence so its median time to fail remains constant for all voltages. The other models show no voltage dependence until the voltage exceeds V_{crit}. Beyond V_{crit}, the V-power and V-exp models have different shapes. The coupled V-exp model has a yet different shape owing to the parameters chosen. Its coupling to temperature is not displayed here since the temperature is constant for the plot. At a different temperature, the coupled V-exp model would change in relation to the other models that are not coupled to temperature. The model parameters of these three voltage-dependent models were chosen here for illustration purposes to provide a median time to fail of $t_{50} = 10^6$ hours at a drain voltage of about 60 V. Of course, in reality the model parameters would be fitted to lifetest data.

At this time, it is believed that one or the other of these proposed models is suitable for fitting most published lifetest data and for predicting failures in GaN HEMTs. It is not clear whether all GaN HEMT fabrication processes actually have this voltage-accelerated mode. In some devices, a clear transition occurs at the critical drain voltage V_{crit}, where these effects come into play. Above V_{crit}, the failure rate appears to abruptly change. This is believed to be caused by a piezoelectric strain induced above V_{crit} that generates dislocations and traps and degrades the characteristics (Joh, 2006-8).

In other HEMT processes, the transition to a voltage-accelerated mode is gradual and there is no specific critical voltage that can be defined. This effect has been likened to TDDB (time-dependent dielectric breakdown) in MOS gate insulators (Marcon, 2010). However, it is not certain whether an actual breakdown ever occurs—rather than a gradual increase in leakage or a gradual current collapse—so long as the voltage is below the sudden catastrophic drain breakdown voltage. When there is no specific V_{crit} but a continuous voltage dependence exists, the above models are still useful by setting V_{crit} = 1 V in Eqs. (3-2) and (3-3) or setting V_{crit} = 0 in Eq. (3-4).

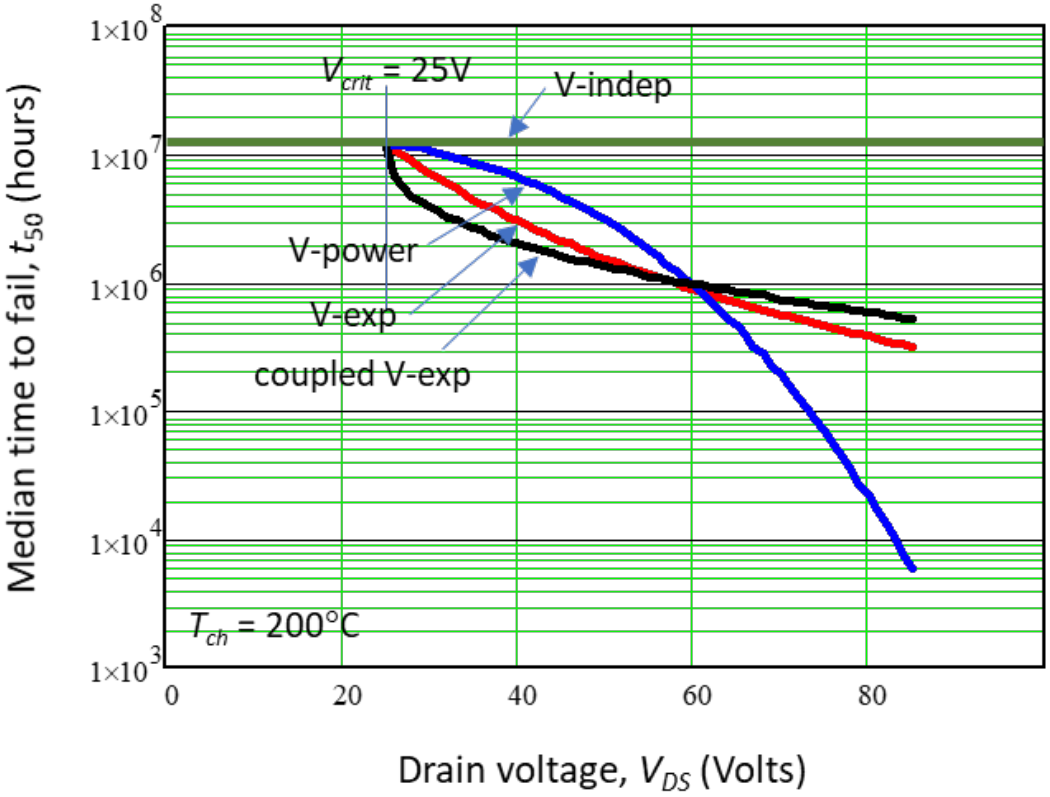


Figure 3-2. Voltage dependencies of four proposed model types.

3.3 DC HEMT Accelerated Test Scheme

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
60 typ 30 min	3	once	✓	✓	✓	Q1, traditional hi power condition
60 typ 30 min						Q2 high current / low voltage condition
140 typ 70 min						Q3 low current / high voltage condition (“semi-on”)
140 typ 70 min						Q4 off-state
Total 400 typ 200 min	3	once	✓	✓	✓	• four Q-points • Special device configs. for temperature estimation desirable (see Appendix E)

Note # DUTs in Column 1 are to be drawn approximately equally from # Lots in Column 2.

A full determination of the model parameters of Section 3.2 requires a series of DC-accelerated lifetests (where the conceptual leap replacing full RF-accelerated testing with DC-only testing has been accepted). The stress conditions must be chosen judiciously. It is recommended here that a determination of the value of the critical voltage V_{crit} first be determined (see Section 3.4 below) prior to commencement of

DC lifetests. The Q-points Q1 and Q2 lie below the critical voltage and require only thermal accelerations—temperature-accelerated lifetests (TALT). The appropriate time-to-fail model is shown in Eq. (3-1). The Q-points Q3 and Q4 require a combined thermal and voltage acceleration approach.

Choosing the stress conditions for the four Q-points requires a strategy as summarized in Fig. 3-3. In this figure the scheme for the accelerated testing strategy is represented. The starred points represent test conditions, with a subset of the available samples devoted to each. For the Q-points Q1 (maximum power and thermal gradient central in the IV plane) and Q2 (high current and low voltage), multiple accelerated temperatures are required at fixed selected voltages. For these two Q-points, the voltage should be selected below V_{crit}. For the Q-points Q3 (high voltage, low current a.k.a. "semi-on") and Q4 (high voltage, zero current off-state), a combination of accelerated voltages and temperatures is required to flush out the model coefficients. Here it is assumed that the existence of a V_{crit} for the device or process has been identified. (If not, then only thermally accelerated tests at selected voltages are required for Q3 and Q4).

The Q3 and Q4 scheme shown in Fig. 3-3 is one of many possibilities for multiple temperatures and voltages. Here it is assumed that the array of test conditions is identical for Q3 and Q4; however, this need not be a requirement. The Q3 and Q4 points shown by the 5-pointed stars are appropriate if the voltage effect is independent of the temperature effect as in Eqs. (3-2) and (3-3). If there is an interaction effect between the voltage and the temperature as described in Eq. (3-4), then additional Q3 and Q4 points are required, as suggested by the 4-pointed stars in Fig. 3-3. A different pattern of test points may be more appropriate, such as an "×" or "+" arrangement, one of the Taguchi DOE (design of experiment) schemes, or even the complete 3 × 3 matrix.

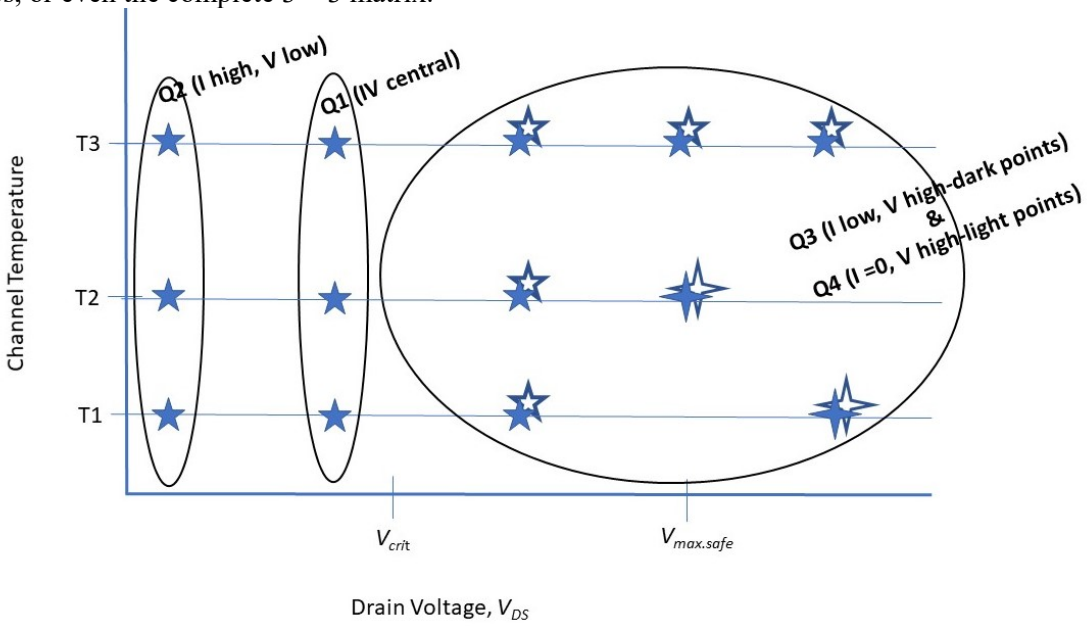


Figure 3-3. Scheme represented in the temperature vs. voltage plane for selection of DC stress conditions. Quiescent points Q1 and Q2 require only multiple temperature-accelerated lifetesting (TALT) at chosen voltages (below V_{crit}). Quiescent points Q3 and Q4 require multiple temperatures and voltages—a combined TALT and VALT (voltage-accelerated lifetest). Q3 and Q4 test conditions are shown as being mirrored for simplicity with the dark points for Q3 (semi-on) and the light points for Q4 (off-state).

For each stress condition point of Fig. 3-3, a sample size of 5 to 10 burned-in parts at each temperature/voltage condition is recommended. This requires 100–200 burned-in DUTs if Fig. 3-3 is fully implemented as indicated. It is possible that fewer test conditions will be required if a voltage dependence

is not found or if V_{crit} does not exist. If any failures occur, the exact causes should be determined using physical failure analysis techniques. The DUTs should be drawn from three lots of wafers.

In each stress, the temperature(s) should be made as high as possible. For the Q1 point stress condition, the channel temperature will be considerably higher than that for the Q2 or Q3 points by virtue of its high DC power dissipation. For points Q2 and Q3, a channel temperature equivalent to Q1 may not be readily achievable. For the off-state point Q4, the channel temperature is identical to the baseplate temperature since there is essentially no power dissipation. In these cases, it may be desirable to elevate the baseplate temperature as much as possible. The maximum baseplate temperatures may be limited by the die attach eutectic solder for points Q2, Q3, and Q4. It is recommended that a higher temperature die attach solder be considered in these cases if possible for reliability testing purposes. Another possibility is to perform the Q2, Q3, and Q4 tests at the wafer level so that packaging and die attach considerations are no longer a concern. The die temperature should be raised to as high a temperature as feasible. Note that this maximum temperature must be compatible with the DC probes or fixtures used. The maximum temperatures should be kept below the temperatures of the final processing or annealing steps for the wafers so as not to engender physical changes not realistic under usage conditions.

Another pitfall sometimes encountered with high temperatures in TALT is that competing noncredible failure modes can sometimes be induced (Gajewski, 2014). These failure modes might not actually occur in usage but are an artifact of the very high temperature acceleration. The typical signature of such noncredible modes is that the failure time distribution becomes bimodal. Atypical early failures may be due to defects or have a very high activation energy. To eliminate defects from the TALT, a burn-in is recommended prior to TALT. When the early failure mode has a very high activation energy level, its presence may not be felt in normal operation and can be eliminated from consideration.

Comparing the DC and pulsed IV characteristics is a very useful way to check the charge trapping problems that introduce gate- and drain-lag phenomena in GaN HEMT devices. Normally, a pulsewidth of 100 nsec to 1 msec is suitable to investigate the trapping problems with sufficient accuracy. The lag phenomenon results in a difference in the drain current for long versus short pulses, related to the trap energy and spatial distribution. The measurement precision of the instrumentation must be adequate to discern this difference. We recommend nominal pulsewidths of 1 μsec (fast) and 10 msec (slow) in the testing sequences described below; however, these pulsewidths may be tailored to better characterize the device and optimize measurement accuracies.

The high field near-pinchoff operating point Q3 is capable of generating hot carriers. Hot carriers can slowly degrade the gain of a device, its threshold voltage, and its drain current. Since a device can enter this regime in a typical pulsed microwave application, it is important that any long-term degradations are understood. In some cases, rebiasing the device to compensate for threshold voltage shifts can recover lost gain. The high field off-state operating point Q4 can introduce piezoelectric strain. Sometimes this strain is called the “inverse piezoelectric electric effect” (IPE), a term that seems to imply something other than the typical electric field-to-mechanical strain coupling that occurs in certain material systems. The high electric field, maximized in operating condition Q4, produces a strain that can cause surface pitting or voiding as the material accumulates vacancies to relax the applied strain. Since many operational scenarios involve a device in the off-state for considerable periods of time, it is important to determine the degradations that may result in this mode. Both Q3 and Q4 lie above V_{crit}, which should be determined first. The challenge is to generate reliability predictions using tests in laboratory times (days to weeks to months) that can be used to extrapolate to satellite mission durations of 10–15 years.

Prior to entering the qualification testing proposed below, the application usage channel temperature and the usage die baseplate temperature should be preselected. These temperatures are needed to define the usage or mission conditions. The channel temperature should be assessed using a combination of

electrothermal modeling coupled with measurements. A wide range of techniques for channel temperature estimation have been proposed, such as the gate line resistance method, electroluminescence, Raman surface probe method, scanning tunneling microscopy method—all accompanied by simulations. Many of these techniques are reviewed in Appendix E. The channel temperature rise is sometimes more complex than can be described by a single thermal resistance value. This is because the heat generated in the active GaN region must diffuse through the GaN-substrate interface. The substrate (commonly SiC) is not lattice matched to GaN, and the "thermal boundary resistance" is not easily modeled (Manoi, 2010). Therefore, the channel temperature measurements are important for reliability projections. Furthermore, the thermal resistance may be highly temperature dependent. At the highest accelerated test temperatures typical in GaN, the effective thermal resistance from the channel to the reference baseplate (or die backside) can be double or even triple its value at usage temperatures. It is important to take this into account in accelerated testing.

Typically with a SiC substrate, the thermal resistance increases approximately proportionally to $T^{1.5}$. The thermal resistance also can be dependent upon the exact location of the Q-point in the IV plane. Consider two Q-points, both dissipating the same power. One Q-point has high voltage and low current, while the other has low voltage and high current. In GaN devices, the high voltage/low current Q-point will show a higher thermal resistance than the low voltage/high current Q-point. This has been explained by the nature of the region where the power is dissipated near the drain edge of the gate. With high voltage, the electric field profile is more concentrated since the channel is more pinched than with a lower voltage (Si, 2013). The power under the high-voltage case is dissipated in a smaller volume as compared to the low-voltage case. This tends to create a higher thermal resistance for the high-voltage case. Equally important is the fact that in a multifinger HEMT device, the hottest finger will be in the central portion of the device and will tend to fail first. The thermal resistance of the hottest central portion is highest, and to minimize errors, should be used. The effect on lifetime predictions of making small temperature errors in TALT is covered by Heller (2008).

Even more complex is the "hot phonon" effect (Choi, 2013; Morkoc, 2012). At the drain edge of the gate, the electric field creates hot electrons over a small region of space. The hot electrons lose energy to the lattice primarily by creation of longitudinal optical phonons. These "hot phonons" have a certain lifetime estimated to be approximately 400 fs, at which point they decay into acoustic phonons. It is the acoustic phonons that are capable of moving the heat away from the region into the substrate. Therefore, for the same dissipated power, an accumulation of hot phonons by the high-voltage/low-current Q-point will raise the effective thermal resistance to a higher value than the low-voltage/high-current Q-point. Despite identical power dissipations, the temperature rise at the high-voltage/low-current operating point may exceed that of the low-voltage/high-current operating point.

Different regions of the IV plane have different thermal resistance levels for this additional reason. The classic hyperbolic constant power locus in the IV plane having a single thermal resistance value may be incorrect for GaN power HEMT devices. Therefore, the various methods of temperature assessments become very important if reliability extrapolations using the Arrhenius relationship are to be performed. Temperature measurement methods are discussed in Appendix D. For temperature measurements, a special device configuration may be warranted, such as one with reduced or eliminated air bridges, or a single gate finger device. The multiple Q-points scheme described here could reasonably be described as "brute force" methods. On the other hand, all the stressing is performed under DC conditions, which is a great luxury compared to performing RF-driven tests under multiple conditions. Using probability plots, maximum likelihood analysis, regression analysis or graphical analysis, the coefficients of the models of Eqs. (3-1) and (3-4) may be determined. The statistical distribution of failure times may be assumed to be lognormal or Weibull as is usual practice, and verified by the use of probability plots or Q-Q plots. The techniques for analysis of statistical reliability test data as described in the JEDEC standard JESD91A (2016) or in the NIST/SEMATECH e-handbook (NIST 2012) are recommended.

3.3.1 Example HEMT Temperature-Accelerated Lifetest Data

Some preliminary data for a GaN RF power HEMT is presented here for illustration of the multiple Q-point scheme. Figure 3-4 shows some typical summary test data in the form of an Arrhenius plot showing the median times to failure (MTF, or t_{50}, denoting the times by which 50% of samples have failed) versus inverse temperature. Packaged samples of one particular GaN HEMT were stressed at the recommended four DC Q-points. Temperatures were estimated using the published values of the thermal resistance and were controlled by adjusting applied DC power with devices on a hotplate. At various times, the stress was interrupted, and RF power measurements were performed at ambient temperature and usage compression of 3 dB. The failure criterion was a decrease in the 3 dB compressed RF power output by 0.5 dB. The projected MTFs vs. inverse temperature for the four recommended DC Q-points are shown on this plot.

Note that all these Arrhenius projections to the mission temperature of 200 °C lie well above even a 15-year mission duration. However, this offers only small comfort since these t_{50} lines represent an estimate of 50% of the population failing—not a particularly worthwhile metric. More useful is to show that the t_{50} projections exceed 1 million hours, which usually provides adequate reliability for most missions.

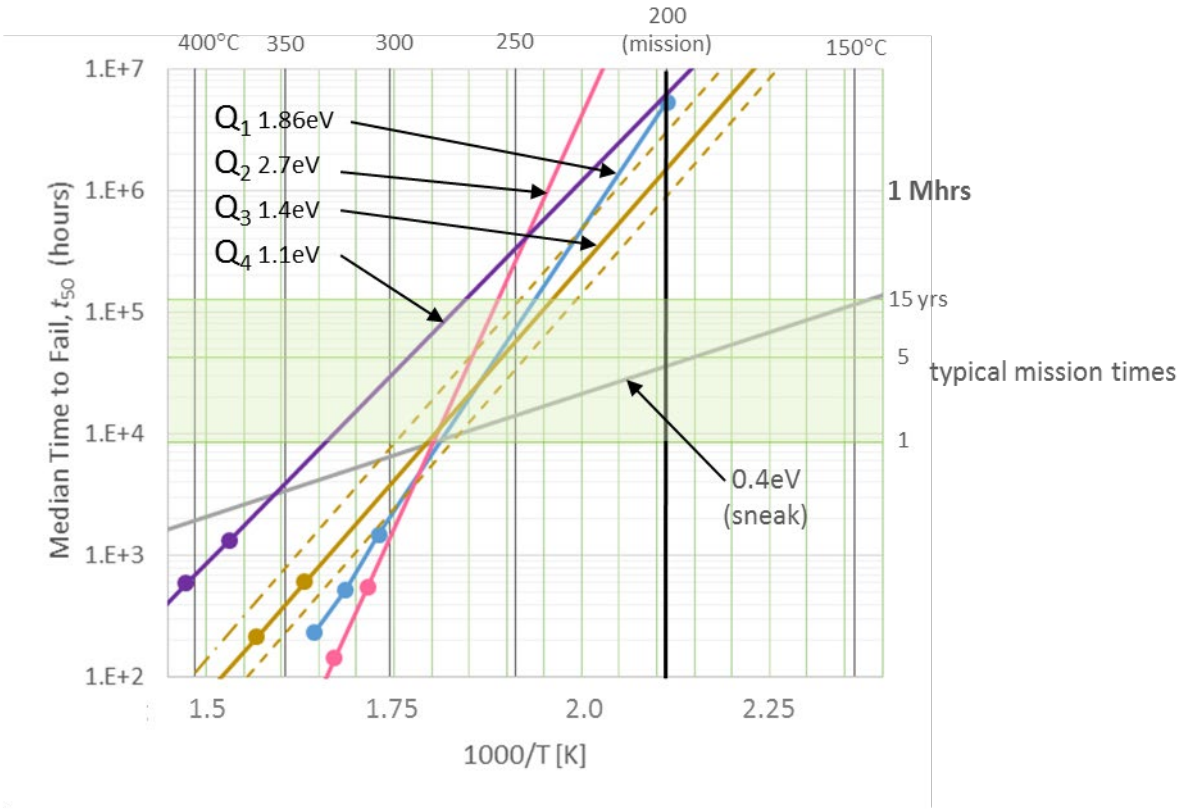


Figure 3-4. Example Arrhenius plot showing temperature-accelerated lifetest (TALT) data points (circles) for the four Q-points and extrapolations to the mission channel temperature of 200 °C.

A summary of the test conditions and resulting activation energies in Fig. 3-4 is as follows:

Q1 max power	V_{DS} = 20 V	3TLT	T_{ch} = 305, 320, 335 °C	E_A = 1.86 eV
Q2 max current	V_{DS} = 5 V	2TLT	T_{ch} = 310, 325 °C	E_A = 2.7 eV
Q3 semi-on	V_{DS} = 50 V	2TLT	T_{ch} = 340, 365 °C	E_A = 1.4 eV

Q4 off-state	V_{DS} = 50 V	2TLT	T_{ch} = 380, 405 °C	E_A = 1.25 eV

The large variation in the extracted activation energy for each of the bias conditions attests to the multiple mechanisms at work. Of each of these four Q-points, the Q3 semi-on condition poses most of the reliability risk at the usage channel temperature of 200 °C. It has the lowest t_{50} projection, at 200 °C. Therefore additional voltage-accelerated lifetesting (VALT) was performed under semi-on conditions at V_{DS} = 40 V and 60 V spanning the initial voltage condition, and with the drain current adjusted to maintain a channel temperature of 365 °C. (Previously, the value of V_{crit} was determined to be approximately 25 V so all tests in the Q3 semi-on condition potentially reflect a voltage dependence.)

The reason that the semi-on or Q3 operating point has the poorest reliability at the mission temperature is not known at this time. It is possible that this particular device is sensitive to hot electrons that damage the region adjacent to the gate-drain edge. Another possibility is that charges accumulate in the passivation at in the drain access region increasing the on-resistance and creating performance degradation. More work is needed to identify whether this is a common trait in other devices, and more physical analysis and more perceptive measurements are needed.

Figure 3-5 explicitly shows that a voltage dependence is found for the Q3 semi-on condition VALT at T_{ch} = 365 °C. It shows the t_{50} values under the accelerated conditions plotted versus voltage rather than inverse temperature. The V-power model of Eq. (3-2) was chosen to fit this voltage dependence giving a power coefficient $n \approx 3$. The same information is shown in an equivalent way by the dashed lines on the Arrhenius plot of Fig. 3-4 spanning the 50 V condition. For completeness, a similar VALT at the off-state condition of Q4 would be recommended.

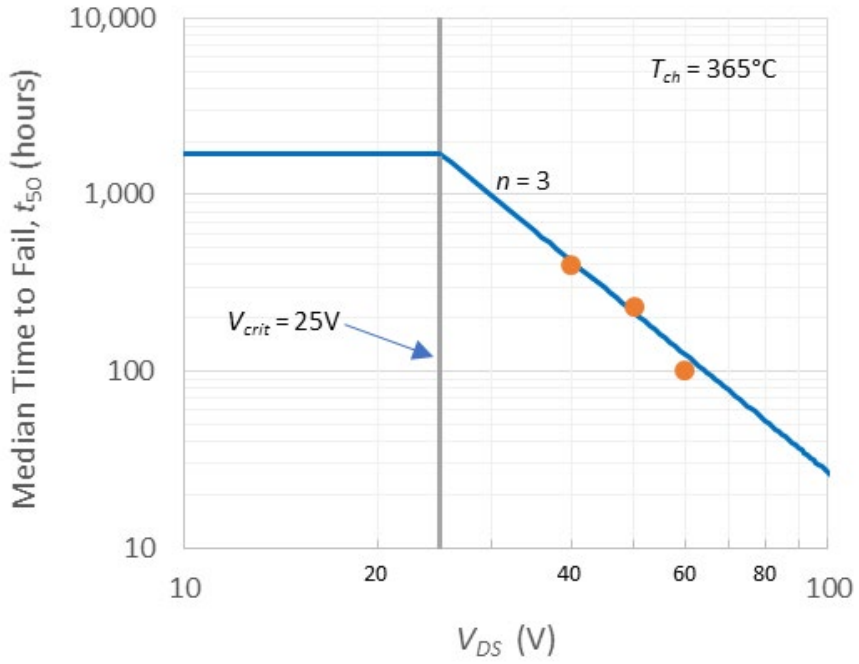


Figure 3-5. Voltage-accelerated lifetest results at constant temperature T_{ch} = 365 °C at semi-on operating point Q3 with three stress voltages, and simple piecewise power-law fit.

3.4 Step Stressing and Critical Voltage Determination

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
8 for TSST	2	once	✓	✓		2 DUTs, from two lots × 4 Q-points
5 for TSST	5	once	✓	✓		1 DUT from each of 5 batches of starting material at Q3

When performing temperature-accelerated lifetests (TALTs) or voltage-accelerated lifetests (VALTs), a practical goal is to perform the tests to generate failures in laboratory times—typically a few hundred hours or a few months at most. The results will then be extrapolated to much longer satellite mission durations, as long as 15 years. Normally "failure" represents a change in a parameter beyond a certain criterion value (a change in P_{out} of 0.5 dB, for example) rather than a complete catastrophic failure. Because of the nature of the multiplicity of failure modes in GaN devices, it may happen that both parametric failures and catastrophic failures occur, there being a mixture of failure modes. Catastrophic failures occurring at extremely high acceleration levels may not represent credible failure modes in normal usage applications. It is highly recommended that, before dedicating resources and DUT quantities to performing TALTs or VALTs, a simple temperature step-stress test (TSST) or voltage step-stress testing (VSST) procedure first be carried out on a small number of devices. Also, step stress testing can help identify the temperatures and voltages that are reasonable for later TALT or VALT. These are considered "pilot" tests to be conducted before beginning a long VALT or TALT test campaign under constant stress conditions.

Temperature step-stress testing (TSST) is recommended at each of the four Q-points identified in Fig. 3-1. Deviating slightly from the JEDEC standard (JEP-118A, para. 4.2, 2018), it is recommended to start at a channel temperature of 150 °C and to perform temperature steps of between 5 °C and 25 °C. The size of the temperature step is dictated by the anticipated activation energy. For high activation energy > 1.5 eV, fine temperature steps of 5 °C are recommended. For low activation energy, a larger step size of 15 °C or higher may be satisfactory. Each step should have a duration of 18 hours' minimum overnight stressing, with cooldowns and interim DC and RF measurements performed during the daytime. Longer or shorter stresses are also reasonable. The interim measurements should be performed at a fixed reference temperature performed at the end of each step. The reference temperature may be room temperature, or a convenient elevated temperature less than or equal to 150 °C. It is recommended to perform this test on 2 DUTs at each of the four Q-points, for a total of 8 samples.

If there is a dominant thermally activated failure mode at a particular Q-point, it may be manifested by a clear increase in degradation beginning at a particular temperature step. A method for estimating the activation energy for a single dominant failure mechanism by temperature step stressing a single device is given in (Yeats, 1997). However, when multiple failure modes exist, as may be the case in GaN HEMTs, this method may not prove to be as useful. A combined RF stress along with temperature step-stressing approach (Paine, 2012a–c) may also be useful in correlating signature DC parameters to RF operation.

Voltage step stress testing (VSST) is also recommend. In many GaN processes, a HEMT can exhibit gradual degradation of performance if the drain voltage exceeds a crititcal value V_{crit}. It is sometimes (not always) accompanied by an increase in gate current. This has been attributed (Joh, 2007-9) to an increase in strain caused by the electric field in the gate-drain region (the so-called "inverse piezoelectric effect," IPE). The strain generates traps or crystallographic defects in the AlGaN or at the 2DEG at the AlGaN/GaN heterojunction. These traps cause increased leakages, a reduction in the transconductance g_m

and an increase in intrinsic drain resistance R_D. The value of V_{crit} depends upon the device geometry, the built-in strain of the starting epitaxial material, the pre-existing trap density, and other factors. Being a mostly electrically originated effect, it may be weakly thermally activated with a relatively low activation energy. In many other devices, there appears to be no critical voltage but rather a continuum of voltage-dependent degradation. In such cases the voltage step stress and VALT are still needed to uncover the voltage dependency. This can be likened to time-dependent dielectric breakdown (TDDB) in insulators, although it is a performance degradation rather than a breakdown that is of interest.

In some GaN technologies a catastrophic short of the gate occurs after a period of time at high-voltage stress. The gate current does not gradually increase before the failure (in fact sometimes it gradually *decreases*). In those cases, there is no threshold or V_{crit}. Instead, a true time-dependent dielectric breakdown is responsible for the degradation of the gate diode. A V_{crit} definition is therefore dependent on the time spent at the stress voltage.

It is recommended that the existence of a V_{crit} be searched for by means of voltage step-stressing. A "semi-on" bias condition is recommended, such as 30 mA/mm, and the drain voltage is stepped up incrementally (Burnham, 2017). The gate voltage V_{GS} is adjusted on each step to keep the drain current constant. It is recommended to step-stress the drain voltage from a starting low value at a baseplate temperature of 150 °C. Alternatively, if the maximum anticipated usage channel temperature is known, step stressing should be performed at that channel temperature. If it is established that a voltage mechanism exists, it is also recommended to follow with voltage-accelerated lifetest (VALT) at multiple voltage and temperature conditions to quantify the voltage-activated failure times.

Note that the voltage step-stress testing (VSST) recommended here is quite different from that frequently presented by others (Joh, 2006-8; Marcon 2010 & 2013; Meneghini, 2011). Here the recommended procedure in this guideline is to step the drain voltage V_{DS}. On the other hand, these authors step the reverse gate voltage V_{GS} to very high values (such as $V_{GS} < -50$ V or more) while holding the drain voltage at $V_{DS} = 0$. This condition is quite unlike normal HEMT operation in an RF amplifier and may lead to errors in the interpretation of the critical voltage. The strain-induced traps that are created when $V_{DS} = 0$ are likely under the entire gate. However, in normal operation, the traps are more likely to occur near the gate-drain edge and in the drain access region.

Figure 3-6 shows an example voltage step-stress test result on a HEMT test structure. The drain steps should be 1 V each and 24 hours in duration. The baseplate temperature during stressing should be adjusted slightly downward in successive steps to maintain the channel temperature fixed as its power dissipation increases if necessary. It is also recommended to adjust the gate voltage at each step to maintain the drain current at the semi-on condition of 30 mA/mm. Following each step, a short characterization of the gate leakage current is performed, along with measurements of transconductance, and gate voltage. Figure 3-6 shows the change in the DC drain current measured at the end of each 24-hour step at the conditions of $V_{DS} = 10$ V and $V_{GS} = -0.6$ V. The criterion for degradation is the abrupt change in the drain current seen once V_{crit} is reached.

This measurement may also be performed on a MMIC rather than on transistors. The MMIC must have independent gate and drain bias pins to permit voltage step stressing and measurements. If the MMIC has multiple stages, they should be measured separately, assuming separate bias pins are provided, or special care must be taken to ensure the stages are biased identically.

Since V_{crit} may depend heavily upon the pre-existing state of mechanical strain in the starting material, it is important to sample devices fabricated from different batches of starting material. It is recommended here to perform this measurement on 5 DUTs each from 5 different batches of starting wafers. This enables the range of V_{crit} to be measured.

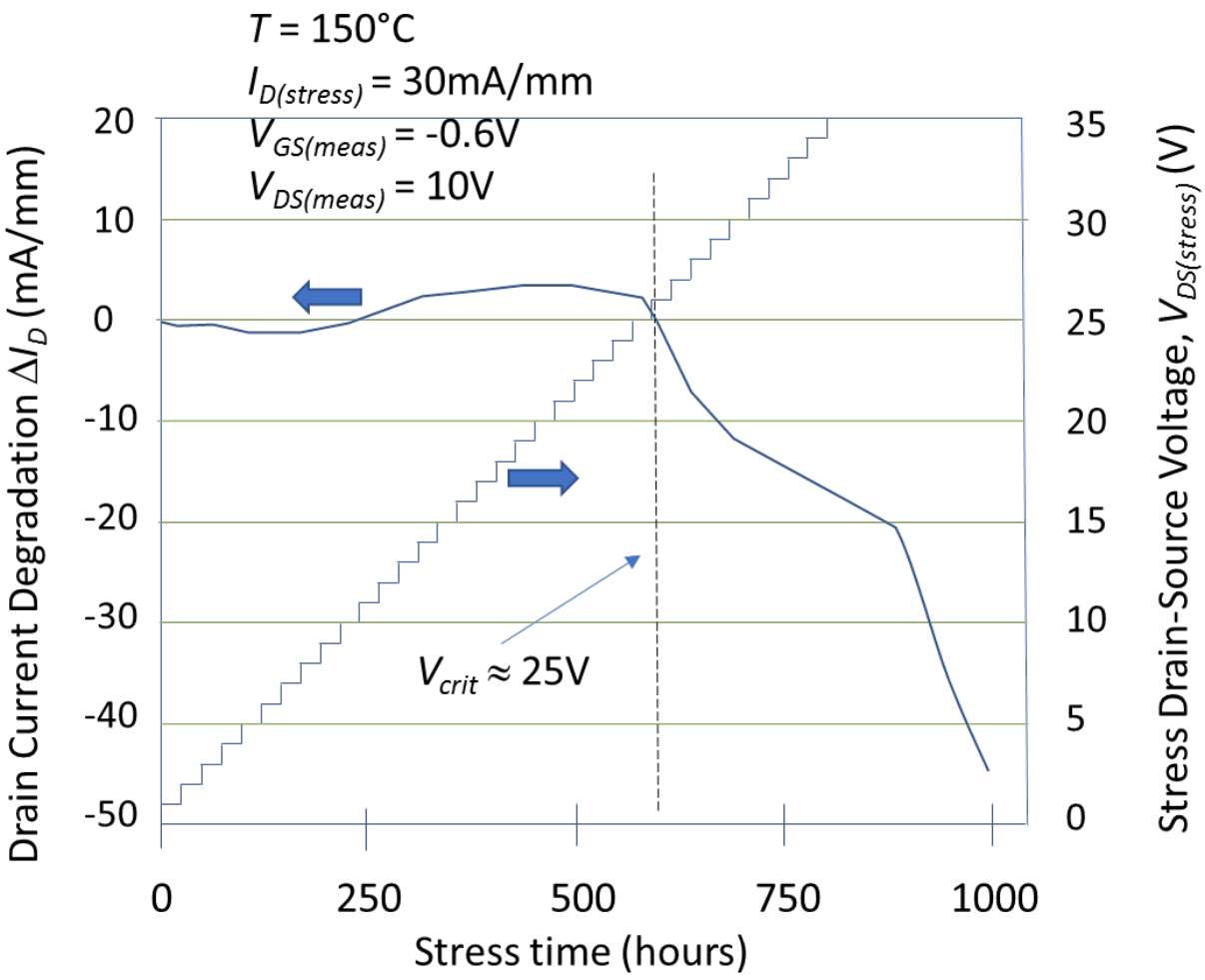


Figure 3-6. Example voltage step stressing test result for drain current degradation in a HEMT. This test is used to determine the critical voltage V_{crit} above which time-dependent degradations begin to occur.

3.5 Recommended Interim Measurements

At various intervals during TALT, VALT, TSST, or VSST, the following room temperature nonstressing measurements and accompanying failure criteria are recommended. It is necessary to stop any high-temperature stressing, cool down to room temperature or to a defined intermediate temperature, and execute a series of interim measurements. The test setups as described next are recommended for performing the interim measurements.

3.5.1 Basic IV Measurements

Basic current-voltage (IV) measurements of GaN HEMTs or MMICs can be made using a semiconductor parameter analyzer (SPA) for DC characterization. An SPA has sources that can be ramped or stepped in voltage while simultaneously measuring the currents. This is convenient in generating parametric DC IV curves. Unfortunately, GaN RF and microwave devices have significant gain at high frequencies and may oscillate and be damaged unless precautions are taken. An RF or microwave fixture with bias tees, high frequency terminations, and stability networks are usually needed, as shown in Fig. 3-7a. Wafers or mounted die may be probed with impedance-matched probes, replacing the RF fixture. In order to access

high-power regions of the IV plane without significant joule heating that distorts the IV curves, either a pulsed IV (PIV) system or dynamic IV analyzer (DIVA) is needed (Tsironis, 2009). Using pulsed sources with low duty cycle, the IV curves can be taken over extended ranges of voltage and current. In Fig. 3-7a, replacing the sources with pulsers can cause additional difficulties. It is often not possible to apply pulsed signals through typical bias tees, as their time constants may be relatively long. Special high-speed bias tees are available that can pass microsecond high-current pulses at the bias ports. An alternative to a bias tee is a pair of back-to-back 90° microwave hybrids to separate the pulse and RF paths. The hybrids must have the correct bandwidth to be compatible with the DUT and have sufficient current carrying capacity. Other approaches that switch out the bias tees while the DUT remains in a stressing setup—minimizing handling—have also been proposed (Paine, 2017).

The setup as described in Fig. 3-7a may not always be suitable for certain measurements. For example, in measuring the gate leakages or subthreshold slopes in a HEMT or MMIC, the bias tees or the stabilization networks may leak more current than the DUT. As long as the device is biased off, or at relatively low current, its RF gain or transconductance is low and it has less tendency to oscillate. In those cases, the bias tees and stability networks can be removed for low current measurements. Many MMICs have internal stability networks and built-in bias tees, simplifying the test setup greatly.

3.5.2 s-parameter Measurements

Figure 3-7b shows the test set required to make s-parameter measurements of fixtured HEMTs or MMICs. A vector network analyzer (VNA) is used to make the measurements which are swept over the frequency range of interest. The VNA must be calibrated (Keysight, 2014) to remove the effects of mismatches, frequency errors, and directivity errors at the input and output planes of the DUT. An RF fixture or prober is used to hold the DUT, and the entire system must be calibrated to remove the effects of the cables, fixtures, and probes. The DUT is shown here as a general amplifier and may be either a transistor or a MMIC. Bias tees are needed for a transistor, but may not be necessary for MMICs since they may be internal. It is also possible to perform pulsed s-parameter measurements, which may more closely match the mission usage.

3.5.3 Power Sweep Measurements

Figure 3-7c shows a test set recommended for P_{out} vs. P_{in} measurements of a HEMT or MMIC at a single frequency. From a curve of P_{out} vs. P_{in}, the dynamic range of the DUT may be determined along with the onset of nonlinearity described by metrics such the 1 dB or 3 dB compression points and 3rd harmonic intercept point IP3. A VNA is required with a 3rd receiver input port along with an internal algorithm that uses a feedback power leveling loop to control the input power P_{in} to the DUT. If a VNA with this capability is not available, the same functionality can be achieved with a variable-level signal generator, a power sensor to detect the input power, and a spectrum analyzer or power meter to measure the output power.

Figure 3-8 shows an example set of interim performance characterizations of a HEMT or MMIC. The test setups as described above are capable of all the measurements required. Unless otherwise stated, it is recommended to make most of the following measurements using a PIV or DIVA with a relatively short pulsewidth of 10 μs (if bias tees allow, otherwise as short as possible) and duty factor <1%. The Q-point for all of the pulsed measurements should be (V_{DS}, V_{GS}) = (0 V, 0 V).

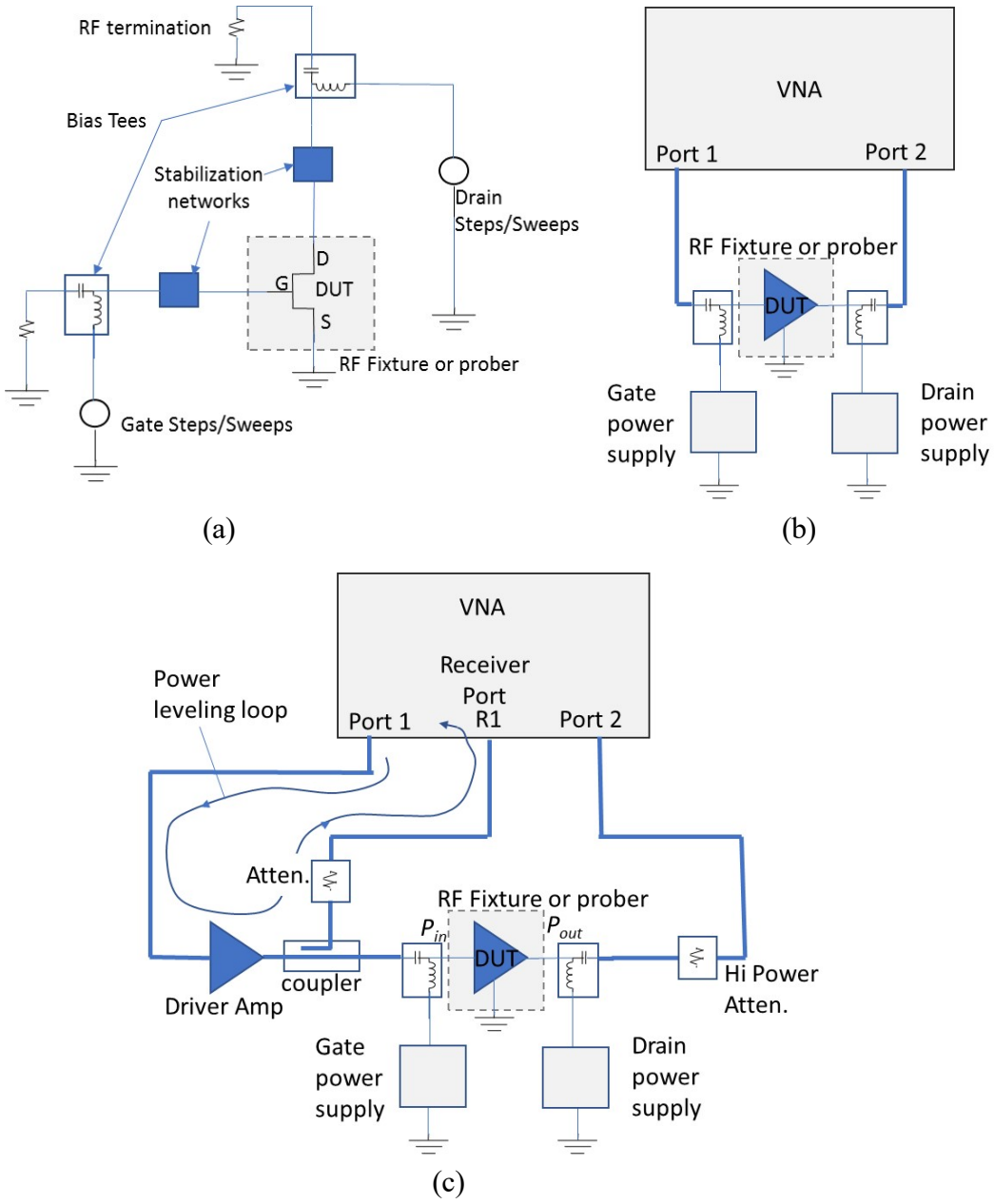


Figure 3-7. Test setups for DC, pulsed and RF measurements, including (a) for measurement of pulsed or DC parameters using SPA, PIV system, or DIVA, (b) basic network measurements (s-parameters) using a VNA, and (c) power measurement setup using a pulsed VNA with RX port.

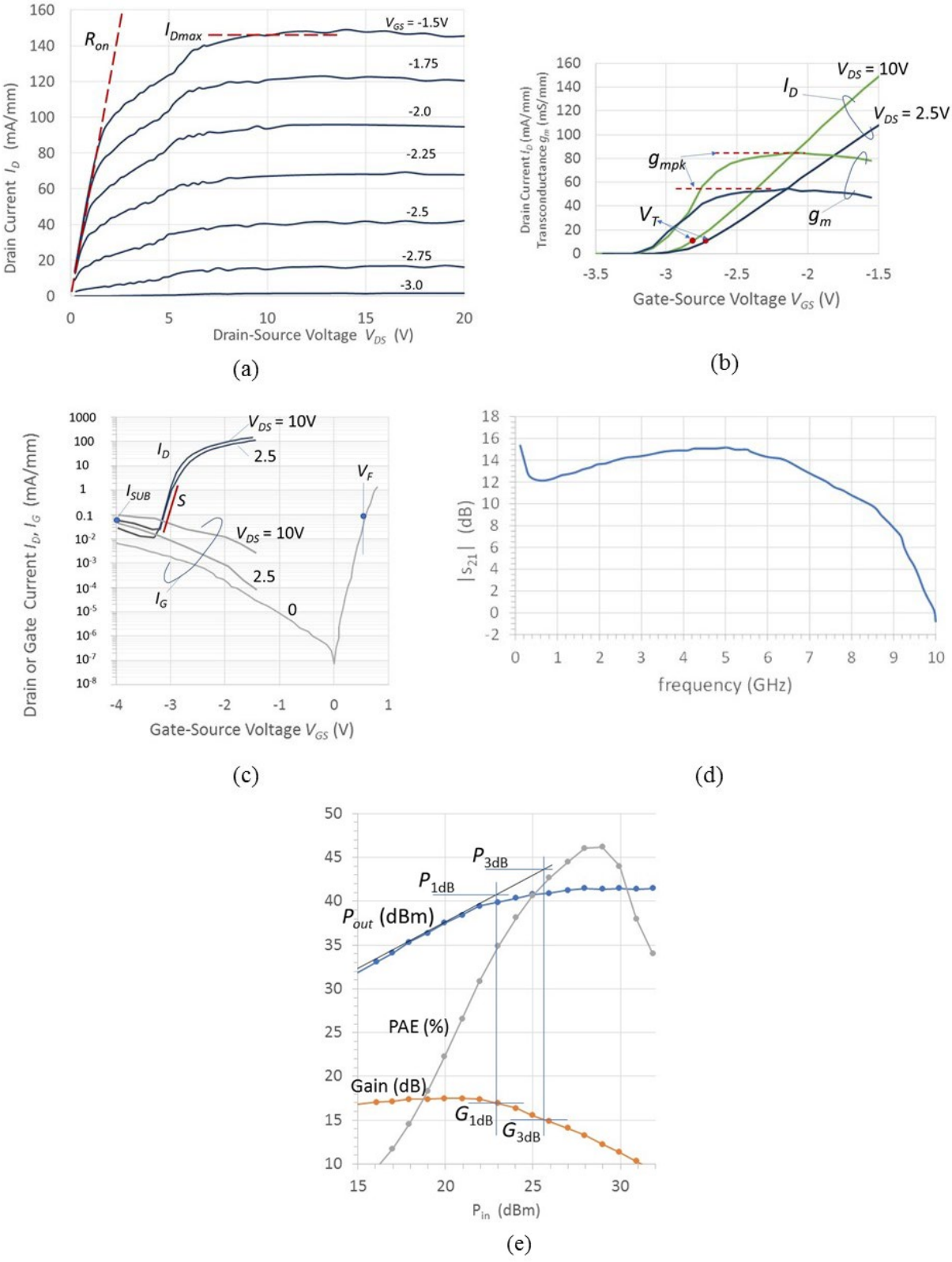


Figure 3-8. Examples of the various interim measurements for reliability tests of GaN HEMT devices: (a) common source characteristics, (b) transfer characteristic, (c) subthreshold drain, forward gate and reverse gate currents, (d) small signal s_{21}, and (e) large-signal power sweep.

From the above measurement and setups, the following device parameters should be extracted and are illustrated in Fig. 3-8.

- Basic IV performance characteristics, PIV system, or DIVA (Fig. 8a)
  - I_{Dmax} maximum drain current at specified V_{GS} and V_{DS}
  - R_{Don}, on-resistance of the HEMT taken as the slope of I_D vs. V_{DS} for V_{GS} = 0 V
  - I_{DSS} drain current at a specified V_{DS} with V_{GS} = 0 V (short pulse to avoid thermal damage)
  - g_{mpk} peak transconductance from transfer curves, fast pulsed
  - V_{th} threshold voltage at defined V_{DS} and I_{DS} taken from transfer curves
- Low- to medium-current characteristics, with device in low-gain conditions allowing the elimination of the bias tees connecting the DUT to SPA (Fig. 3-7a)
  - I_{Dsub} Subthreshold drain leakage current at specified V_{DS} and V_{GS}
  - S Subthreshold slope expressed as mV/decade
  - V_F forward voltage of the gate-channel Schottky diode at specified forward gate current, typically 0.1 mA/mm or 1 mA/mm
  - $I_{F,}$ *f*orward gate current of the gate-channel Schottky diode at specified forward gate voltage, typically between 1 and 2 volts, with V_{DS} = 0.
  - I_G reverse leakage current of the gate diode at specified reverse gate voltage, and drain voltage
- small-signal characteristics, VNA (Fig. 3-7b)
  - s_{21} measured at mission-like Q-point, over mission bandwidth
- large-signal characteristics, VNA (Fig. 3-7c)
  - P_{1dB}, output power at 1 dB compression point at selected bias, frequency, and temperature
  - G_{1dB}, large signal gain at 1 dB compression point at selected bias, frequency, and temperature
  - P_{3dB}, output power at 3 dB compression point at selected bias, frequency, and temperature
  - G_{3dB}, large signal gain at 3 dB compression point at selected bias and temperature
  - PAE (power added efficiency) at selected quiescent bias point and temperature

All the above interim tests described in this section should be tailored appropriately for the DUT in question. Attention should be given to the voltage levels, currents, frequencies, pulsewidths, and power levels that best match the usage conditions of the mission.

Note the inclusion of DC gate leakage current I_G in the list above. It should be pointed out that changes in DC gate current do not usually indicate a failure—it is included here for completeness and for characterization purposes. Unless the gate leakages increase catastrophically (10× to 100× or higher), there has not been much correlation with gate leakage to RF and small-signal performance degradations.

3.6 Other Measurements

It is now recognized that GaN HEMT devices possess characteristics of a dynamical nature related to trapping phenomena. These phenomena are not captured by the largely standard and familiar measurements as just described. It is important to capture the dynamic phenomena especially since they may be directly related to reliability. However, the level of understanding of these phenomena is not

sufficiently established at this time to allow standard test methods and guidelines to be proposed. This is especially true for qualification of GaN HEMT devices for ultrahigh-reliability space missions. Instead, a description of a few not fully standardized measurements and test techniques is presented here to describe the nature of the dynamic behavior of GaN HEMTs.

3.6.1 Pulsed IV / DIVA Dynamic Parameter Measurements

There exists a high density of dislocations and a high trap density even in a fresh device. There may be pre-existing or stress-generated trapping centers under the gate or in the access region of a HEMT. These traps cause various phenomena, such as "drain lag" or "current collapse." These effects occur because as the electron Fermi level changes under the influence of applied voltages, the traps fill or empty accordingly. Traps have certain time constants depending upon their nature and energy level with respect to the conduction band of the semiconductor. These time constants produce the dynamical effects (Tirado, 2007). With aging, particularly with stressing above V_{crit}, the density of the traps may increase, worsening the dynamical effects. In a long mission, a gradual degradation in output power or gain may occur. The measurement of these dynamical effects using a pulsed method capable of determining degradations from increased trap densities (Sasikumar, 2015) may be useful as a possible future standard. The following family of measurement metrics could be defined as follows:

- Dynamical factors, PIV system, or DIVA (Fig. 3-9)
  - $\Delta I_{DSS(\text{pulsed})}/I_{DSS(\text{static}),}$ drain current collapse ratio defined as the ratios of the pulsed drain current to the static drain current for traps empty (QE) and traps full (QF) quiescent points (Fig. 3-9a)
  - ΔR_{Don}, on-resistance changes between pulsed and static conditions defined with the same two Q-points (Fig. 3-9a)
  - $\Delta V_{T\,,}$ dynamic threshold voltage changes defined as shifts measured using pulsed transfer characteristics vs. static characteristics with the same two Q-points (Fig. 3-9b).

Figure 3-9 shows the proposed method of measurement of dynamical effects. A pulsewidth of 10 μsec is recommended, along with a very long pulse repetition period of 100 msec or 1 sec. The PIV or DIVA system is programmed to perform two different measurements, each starting with two different Q-points, for a total of four tests. The two Q-points are a "traps empty" quiescent point (QE), and a "traps-full" quiescent point (QF). The two different measurements are a pulsed I_{DSS} sweep and a pulsed transfer characteristic. The four tests illustrated in Fig. 3-9 are as follows:

- I_{DSS} measurement with pulsed drain voltage swept from 0 V to 10 V (Fig. 3-9a) with quiescent point QE, (V_{DS}, V_{GS}) = (0 V, 0 V)

- I_{DSS} measurement with pulsed drain voltage swept from 0 V to 10 V (Fig. 3-9a) with quiescent point QF, (V_{DS}, V_{GS}) = (20 V, –4 V)

- Transfer characteristic with V_{DS} = 3 V, and V_{GS} swept from –4 V to 0 V (Fig. 3-9b) with quiescent point QE, (V_{DS}, V_{GS}) = (0 V, 0 V)

- Transfer characteristic with V_{DS} = 3V, and V_{GS} swept from –4 V to 0 V (Fig. 3-9b) with quiescent point QF, (V_{DS}, V_{GS}) = (20 V, –4 V)

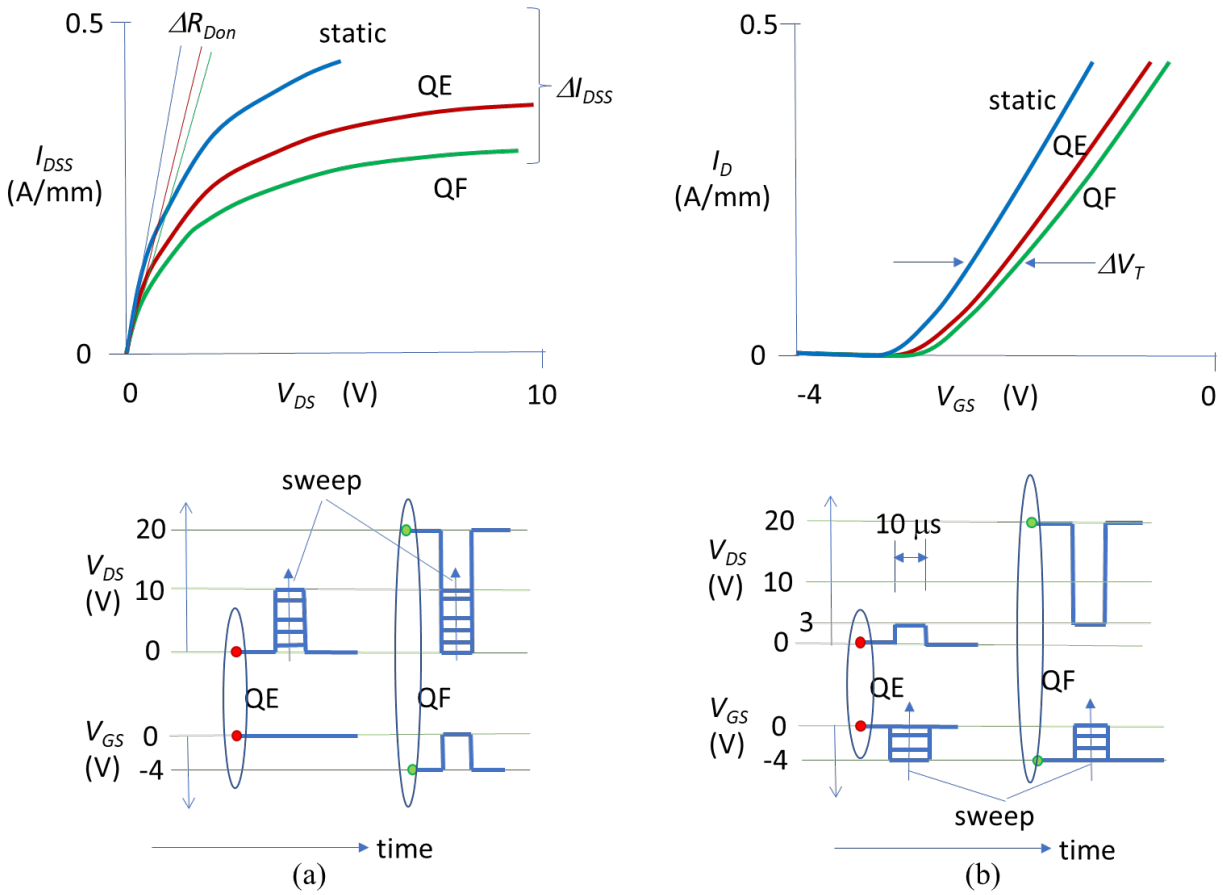


Figure 3-9. Dynamic characterization of trapping phenomena in GaN HEMTs using PIV measurements under two different quiescent states—traps empty state QE and traps full state QF. Figure 3-9a shows PIV plots with the two Q-points as drain voltage is swept, and Figure 3-9b shows PIV transfer curves for the same two Q-points. The drain and gate PIV voltage stimulus waveforms are shown below the plots.

The pulsed voltage waveforms that produce these measurements are shown in Figure 3-9. In addition, the static measurements with a conventional semiconductor parameter analyzer or curve tracer are shown in the figure. The series of pulses are sufficiently short with a sufficiently low duty cycle so that there is insignificant joule heating—a provision that should always be verified. For the two I_{DSS} sweeps, the pulse conditions are identical, but the starting or quiescent points differ. The trap states—empty in the QE case—are filled in the QF case, and therefore the charge state of the HEMT differs. Because the pulsewidth is relatively short, the trapping states in either case are observed unobtrusively. For comparison, the static DC characteristic is also shown. To avoid device destruction, the thermal dissipation must be kept in check when performing the static IDSS measurement. The recommended drain voltage for the pulsed measurements is V_{DS} = 10 V and should be well below V_{crit}. For the static measurements, the thermal dissipation will limit the extent of the characterization. The differences between the static and dynamic characteristics and between the two different dynamic characteristics is an indication of the bias-dependent trapping that affects device performance. The ΔI_{DSS} *and* ΔR_{Don} parameters emphasize the traps that exist in the AlGaN layer near the drain edge and drain access region of the device, since the measurement is taken under a saturated condition.

For the transfer characteristic sweeps, the same two Q-points are employed. The difference in trapping states affects the threshold voltage, as shown in Figure 3-9b. It is recommended to perform the transfer

curve gate sweeps with a low drain voltage such as V_{DS} = 3 V so that HEMT stays in the linear region. Here the static characteristic may be relatively unaffected by thermal considerations since dissipation is fairly low. The state of charging in the region under the gate or in the access region will affect the dynamical vs. static threshold voltages. The threshold shift parameters on the other hand emphasize traps directly under the gate since the pulsed measurements are performed in a linear mode of HEMT operation.

These dynamical measurements are particularly valuable since they could capture in a standardized way the trapping phenomena that cause current collapse and HEMT instability. The pulse period (100 msec or 1 sec) and pulsewidth (10 μsec) suggested here are not incompatible with many applications, such as communications systems or radars. The pulse time parameters may be tailored to the application as needed. For example, to completely fill or empty traps, it may be necessary to employ even lower-duty cycles so that the device remains at QE or QF for many seconds or minutes. This might be necessary in HEMT amplifiers that operate infrequently or in single-pulse mode.

It has been shown that pulse instability caused by the trapping effects can cause significant pulse distortion in certain applications (Tome, 2019), requiring major efforts to compensate. It is unknown at this time whether pulse instability such as this might worsen with aging, usage stress, and radiation in a space environment. If a candidate HEMT or MMIC begins life with a high trap density and has a large pulse instability at BOL, it may not be a good candidate for space usage, especially operated above V_{crit}, where trap density may increase further. On the other hand, a certain amount of current collapse or trapping may be tolerable in a certain application, such as a pulsed RF heavily saturated power application. It would be very important to quantify whether the dynamic current collapse effect or dynamic threshold shift effect worsen with aging or mission life. The dynamic tests and parameter measurements as explained in Figure 3-9 are highly recommended here as practical standards to quantify such phenomena.

Note also that the parameter R_{Don} describes the drain effective on-resistance. This is the parameter most of interest to circuit designers using HEMTs as switches in inverters and switching regulators. These circuits are also used widely in space applications. Here the device acts as a switch being either fully on or fully off. It spends little time transitioning between the two states. Therefore the shape of the IV curves, the current collapse, or the dynamic threshold voltage has little import. This situation differs from that in RF/microwave amplifiers and other circuits aimed at linear or quasi-linear behavior. The other parameters may be much more important (or at least equally so) than ΔR_{Don} in the RF/microwave applications of GaN HEMTs.

3.6.2 Direct Trap Characterization Measurements

It is now recognized that trapping phenomena in GaN HEMTs may limit performance. While the results from dynamic measurement using PIV and DIVA equipment as described just above are ultimately controlled by the traps in a HEMT, it would be more desirable to measure the trapping physical parameters in a more direct way. Various diagnostic methods have been proposed and compared to study the reliability degradation aspects of traps (Tartarin, 2011). However, at this time, there are no standard methods for characterization of traps in GaN HEMTs or MMICs. Further, there are presently no criteria for acceptable trap density, trap energy level, or spatial location of traps commensurate with ultrahigh-reliability GaN HEMTs for space missions. It is believed that traps can degrade the electrical performance when a device is subjected to space radiation.

Bisi (2011) has tabulated a survey of the characteristics of traps seen in GaN devices and materials. Many different trap species have been found, depending upon the material growth, substrate, fabrication

process, and device type. Identification of exactly which traps contribute to which specific electrical performance limitation is a fundamental question. Some indications are that one particular trap level located approximately 0.5 eV below the conduction band in the AlGaN barrier layer is responsible for degradations under RF stress (Sasikumar, 2012). One way to study the traps is with capacitance DLTS (deep-level transient spectroscopy), performed over a range of temperatures, including cryogenic temperatures using specialized instruments and software. This is a research tool and is not practical at this time for reliability qualification testing. DLOS (deep-level optical spectroscopy)—in which a subband gap light source/monochronometer or laser directly excites the traps—is a related characterization method (Arehart, 2010; Yang, 2009). It also has not progressed beyond the laboratory. Yet another method is the I-DLTS (current DLTS) technique that can be used directly on three-terminal finished devices and MMICs (Chini, 2009). The technique is more practical but still requires cryogenic temperatures to extract the trap data. Similar electrical transient methods have been proposed (Joh, 2011; Zheng, 2019) and may be more convenient and more promising toward a standard technique, but still have not yet moved out of the research phase. Chen (2017) has utilized this method to identify the physical locations of the traps. Most of these methods require precision pulse equipment and low temperatures to characterize the deeper traps but are extremely promising. It may be possible in the future to integrate these methods into high-temperature reliability stress stations where the devices maintain RF stability at all times (Paine, 2017) while the device is alternately stressed and characterized. Future effort should be carried out to explore some of these methods. They will surely become necessary as GaN HEMT technologies are employed in high-reliability space missions.

In one sense the modeling of the traps for circuit simulation seems to have outpaced the capability to measure them. The traps can be modeled in a circuit simulation program as a series of RC time constants controlled by a dependent current source (Albahrani, 2019). A nonlinear circuit model for the overall GaN HEMT device including its IV and CV characteristics has been developed (Ahsan, 2017). The extent to which this circuit model must be modified to include aging and radiation at EOL, especially for the traps, has not yet been determined.

3.6.3 Low-Frequency Noise Measurements

The traps in GaN HEMTs can generate electronic noise as they may charge and discharge continuously. This process is called generation-recombination (G-R) noise or random telegraph noise (RTN), where fluctuations in free electrons occupying the traps cause the device conductance, hence device current to vary. Device current variation can be measured as a spectral baseband noise power. For a single type of trap, the spectral distribution of the G-R noise is proportional to the relaxation time τ, showing a low-frequency plateau and a corner frequency $1/\tau$ beyond which the noise falls off as $1/f^2$ (i.e., a Lorentzian spectrum). For many uncorrelated traps with different relaxation times, the resultant spectrum approaches a $1/f$ rolloff. For a material with a combination of many types of uncorrelated traps, and a few dominant traps with particular relaxation times, the spectral shape may attain a $1/f^n$ with one or more bulges where $n \geq 1$. Environmental, DC, or RF stress could alter the level or shape of the spectrum, allowing for possible identification specific reliability failure mechanisms.

The activity of the traps can be observed directly using a low-frequency noise analyzer (for example, Keysight E4727A) with appropriate low-noise fixturing and biasing, in a low-noise environment such as a screen room. Figure 3-10 shows some low-frequency noise measurements of a GaN HEMT before and after stressing under a semi-on condition for 1,000 hours at a channel temperature of 175 °C. In this plot the drain current noise spectral density S_{ID} (A^2/Hz) has been normalized to the DC drain current for the measurement, made in the linear mode. The fresh device shows a nearly $1/f$ characteristic, while the stressed device deviates from $1/f$, indicating the newly formed traps as a result of stress. Measurements

such as these are very useful to characterize traps for GaN HEMT (Rao, 2012). However, they require specialized equipment and expertise.

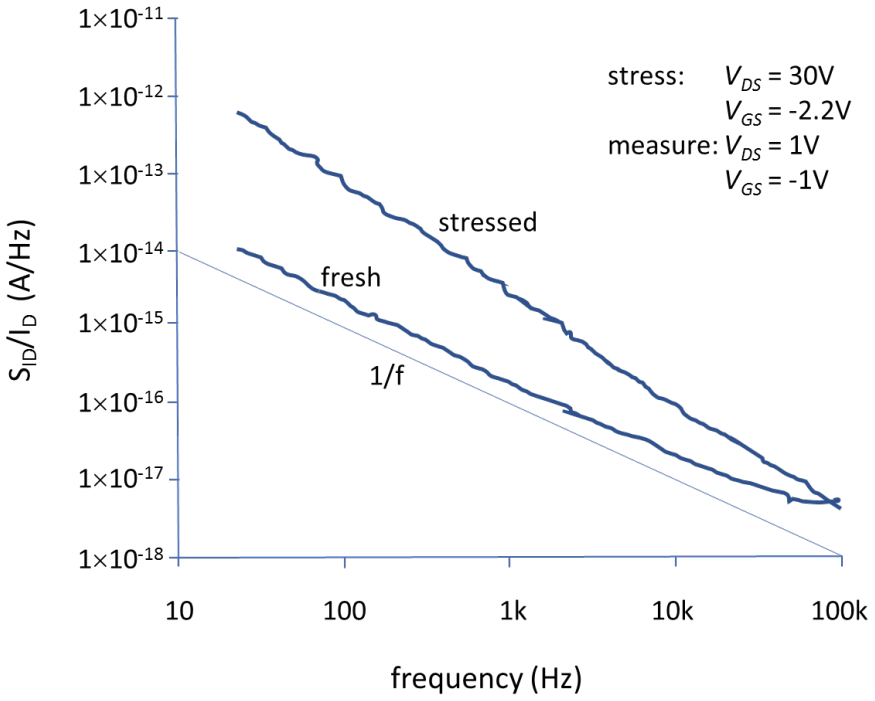


Figure 3-10. Example of a low-frequency noise measurement result on a HEMT before and after stress at 175 °C for 1,000 hours.

3.6.4 Phase Noise Measurements

Compared to baseband low-frequency noise, phase noise has more practical relevance in many RF and microwave applications. Additive phase noise perhaps may be the most critical concern in multicarrier communications systems or pulsed systems (Breitbarth, 2008). The phase noise produced by a GaN transistor or MMIC amplifier is directly related to the trapping phenomena. The additive phase noise can be measured using a technique as shown in Figure 3-11a. A low phase noise RF source is split into two branches, one of which drives the DUT and the other a variable delay line or a variable phase shifter, to create a quadrature signal. When applied to a mixer, the two signals are downconverted to baseband and the RF source phase noise is canceled. The baseband signal therefore represents "residual" phase noise added by the DUT. The results, filtered and displayed on the spectrum analyzer, is the residual phase noise level $\mathcal{L}_\phi(f)$ expressed dBc/Hz, where dBc indicates the noise level is relative to the RF carrier level and is at the frequency offset f from the RF carrier frequency. The results are normalized to 1 Hz irrespective of the measurement filter bandwidth. The activity of the traps in a GaN device injects this noise as modulation or offset from the carrier frequency. If a particular communications or pulsed system requires a high-sensitivity receiver, this noise could degrade system performance. Standard phase noise instruments (for example, the Keysight 5502) can perform these functions, automatically providing a calibrated signal path, making these measurements fairly routine (Faulkner, 1983).

When an input RF signal is applied to a transistor or MMIC amplifier, trap-generated baseband noise is upconverted as both amplitude and phase-modulated sidebands around the carrier. The basic transistor nonlinearities, particularly transconductance and input capacitance nonlinearities, interact with the trap

activity to enhance AM and PM noise as described mathematically by Lee (2005). The phase noise measurement system such as shown in Figure 3-11a provides the phase noise component only. This is often a crucial requirement in a high-sensitivity system.

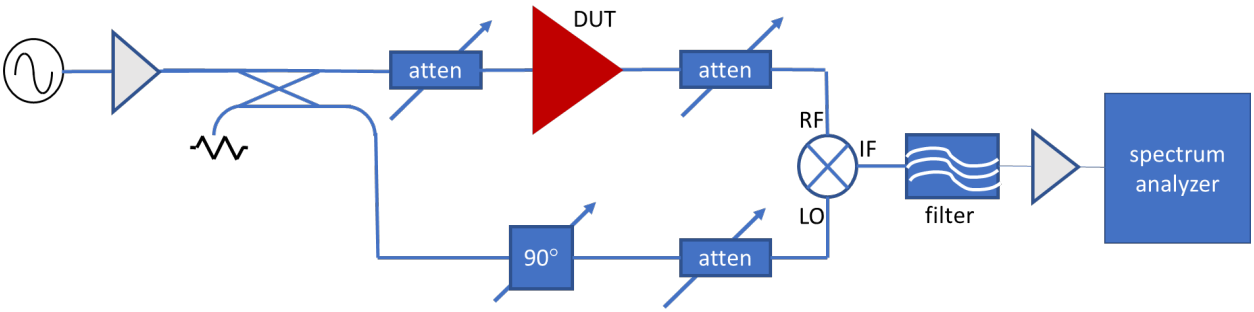
Figure 3-11b shows an example residual phase noise plot of a power GaN MMIC amplifier with a carrier frequency of 200 MHz using a phase noise analyzer. It shows data on a fresh (nonstressed) MMIC under small signal and lightly compressed operation. Under small signal conditions, the device demonstrates a $1/f^2$, $1/f$ and a flat spectrum for the 1–100 Hz, 100 Hz – 1 kHz, and > 1 kHz offset regions, respectively. The plots show the ratio (in dBc/Hz) of the noise power at an offset frequency to the carrier power. Note that the output carrier power level increases markedly by many dB when moving from small signal into compression. Yet all three phase noise $\mathcal{L}_\phi(f)$ measurements in the $1/f$ regime appear to lie atop one another in this figure. This indicates that a particular collection of traps with time constants in the range of about 1–10 msec exist in this HEMT that generate $1/f$ noise. See Breitbarth (2008) for details on interpretation of phase noise measurements.

Since many systems are now being proposed that include not only GaN HEMT power amplifiers but also GaN HEMT LNAs and oscillators, the phase noise question becomes more important. It is recommended that users consider phase noise measurements such as described here for qualification of a GaN HEMT or MMIC as dictated by performance requirements of the system application.

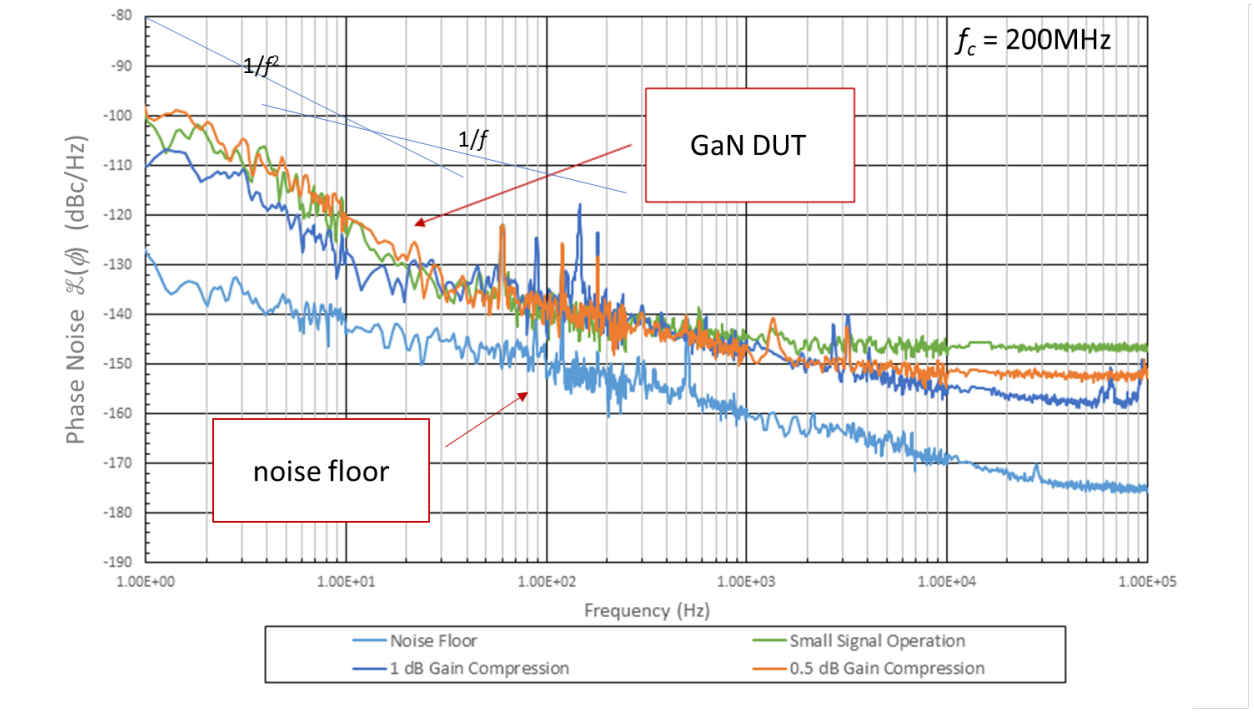
The recommended measurement is of phase noise at a particular offset frequency, such as 1 kHz away from the carrier:

- $\mathcal{L}_\phi(f)$: phase noise level measured at a 1 kHz offset from the carrier, expressed in dB with reference to the carrier output, and normalized to a bandwidth of 1 Hz.

Note that it is possible to specify a different offset frequency rather than 1 kHz or require a phase noise level over series of offset frequencies, as the system usage might dictate. As the device or MMIC is subjected to lifetesting or radiation testing, the changes in noise power spectral density may become important.



(a)



(b)

Figure 3-11. Block diagram (a) of a phase noise measurement system and a typical phase noise plot (b) of a GaN HEMT MMIC amplifier under small signal and compressed conditions (plot courtesy of Chris Clark, Aerospace).

3.7 Failure Criteria

When performing lifetests or step stresses (TALT, VALT, TSST, VSST), a criterion by which to declare a failure is needed. Sometimes multiple failure criteria are needed for different mechanisms, and sometimes these tend to give different lifetimes, activation energies, etc. For the tests described herein, it is recommended that the following failure criteria be utilized for the above measurements:

- Basic IV parameters
  - >10% change in pulsed IV parameters I_{Dmax}, R_{Don}, I_{DSS}, and g_{mpk}

- >50 mV change in threshold voltage magnitude (either a decrease or increase in V_{th})

- Low/medium current characteristics

  - >10× (tenfold) increase in subthreshold and leakage currents, I_{Dsub} and I_G

  - >50 mV change in Schottky forward voltage magnitude (either a decrease or increase in V_F)
  - >15 mV/decade increase in subthreshold slope, S
  - >10% change in forward gate current I_F
    - Note here the DC gate current leakage criterion I_G . While DC gate current usually does not have a correlation with other performance parameters such as the RF degradations listed next, a tenfold increase may indicate a cause for concern.

- RF/microwave small signal and large signal parameters (over the designated bandwidth)

  - >0.5 dB degradation of s_{21} or G_{1dB} for transistors or per amplifier stage
  - >1 dB degradation of P_{1dB} for transistors or for a MMIC amplifier
  - >1 dB degradation of P_{3dB} or G_{3dB} for transistors or for a MMIC amplifier
  - >5% change in PAE
    - Note: For a three-stage amplifier MMIC, for example, it is recommended that a small signal s_{21} or lightly compressed G_{1dB} gain degradation failure criterion of >1.5 dB be utilized—0.5 dB per stage. However, for the same amplifier in saturation, a failure criterion of >0.5 dB degradation in saturated output power P_{3dB} or large signal gain G_{3dB} is recommended. This is because in compression, the last stage is usually the most affected.

- Pulsed IV dynamic parameters

  - >10% change in the drain current collapse ratio, $\Delta I_{DSS(pulsed)}/I_{DSS(static)}$, for both Q-points QE and QF
  - >10% increase in the on-resistance change ΔR_{Don} between static and pulsed conditions, for both Q-points, QE and QF
  - >75 mV change in threshold voltage difference ΔV_T observed between static and pulsed conditions for both Q-points, QE and QF

- Phase noise

  - >2 dBc/Hz increase in phase noise level $\mathcal{L}(\phi)$ at 1 kHz offset from carrier

Utilizing these multiple failure criteria, the time to failure for each of the measurements should be found for each of the four DC stress conditions Q1, Q2, Q3, and Q4 at the two channel temperatures. For any of the above failure criteria, the MTTF shall not be less than 1×10^6 hours at the usage channel temperatures as defined above. Figure 3-12 shows generalized degradations of a parameter measured at various times. The failure times t_{f1}, t_{f2}, and t_{f3} for three individual test samples to reach a 10% degradation are shown. Note that degradations could also be in the positive direction for certain parameters such as the drain collapse ratio $\Delta I_{DSS(pulsed)}/I_{DSS(static)}$ or static drain on-resistance R_{Don}. As degradations are only infrequently linear with time, it is recommended that users attempt to transform the time axis to linearize the data, for example plotting as $t^{1/2}$ or $\log(t)$. It is anticipated that the various physical mechanisms will contribute to different degradation rates in these measurements for the four DC stress conditions. The Arrhenius parameters for the degradation rates of each of the above parameters should be found, with stressing

continuing until all samples have reached the failure criterion. Depending upon the parameter and its activation energy, the failure times may be widely different. Failure of the GaN HEMT as a whole is then defined by the smallest of the various parameter failure times to reach a 10% degradation when extrapolated to the desired usage condition. This is dissimilar to the three temperature lifetests as described in JEDEC standard JEP118A, for example, since other parameters and failure mechanisms may now participate in GaN HEMTs.

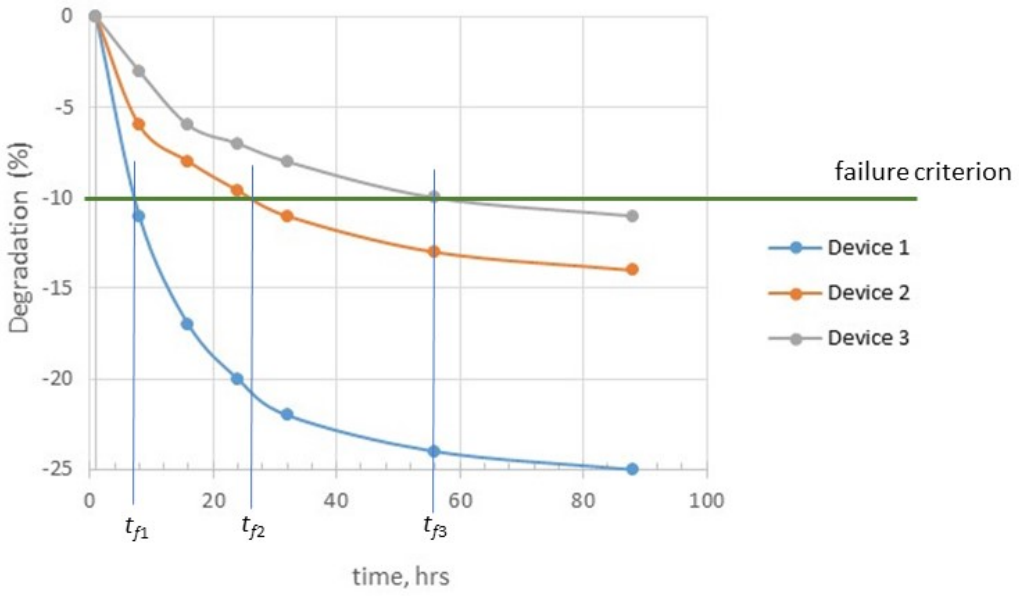


Figure 3-12. Example of degradation of a parameter showing times to failure for three in devices under test.

3.8 Alternate Approach—Signature Parameters (SPs)

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
240 80 min.	3	once	✓	✓		• DC SP tests • 20 DUTs × 3 Temps. × 4 Q-pts • 10 DUTs × 2 Temps. × 4 Q-pts (min)
60 20 min.	3	once	✓	✓		• RF tests for correlation • 20 DUTs × 3 Temps. • 10 DUTs × 2 Temps. (min.)

Unfortunately, there may be cases where the 4-Q-point approach as described in Section 3.1 may provide unacceptable reliability. Or it may be too demanding to require full RF output power measurements to be made periodically to determine degradations. An alternate approach is also possible as explained in detail in (Paine 2015a–c) using "signature parameters." Rather than performing RF output power measurements at intervening times during the DC stressing, it may be possible to use DC measurements only. This enables greatly simplified in-situ tests. However, a single one-time full RF-driven lifetest is then needed to corroborate or scale the signature parameters. Much depends upon the particular details of the mission for this approach to be valid. The idea is that the DC-to-RF correlations are sufficient once correlations

between them are known. The general efficacy of the method, while not fully established, appears promising. A brief summary of this technique is presented below.

It is also possible that the 4-Q-point approach may in some cases be too conservative. During the traversal of the RF loadline during actual use, the device dwells at (or near) any of the 4 DC Q-points only briefly, rather than continuously. Therefore, the degradation engendered by the DC stressing may be much greater than in actual usage with a real RF waveform. The signature parameters approach may help to quantify this effect.

The recommended procedure is to first select (after much initial experimentation, step stressing, etc.) signature parameters that best characterize each of the reliability failure mechanisms that may exist. For example, in Paine (2015b & c) some of the signature parameters, their corresponding failure mechanisms, and activation energies were:

- Δg_{mpk} to characterize hot electron damage at bias point Q1, E_A = 1.1 eV
- ΔV_{th} to characterize electron trapping at bias point Q4, E_A = 0.52 eV
- ΔI_{Dmax} to characterize surface pitting at bias point Q3, E_A = 0.78 eV

Note that other failure mechanisms may also exist with their own signature parameters, but these three are shown here for simplicity. For completeness the missing Q2 quiescent point (low voltage / high current) is added here. It is believed that its most likely signature parameter would be

- ΔR_{Don} to characterize source/drain contact degradation at bias point Q2, E_A not yet known

The change in drain resistance parameter ΔR_{Don} was not discussed by Paine (2015a–c); however, its inclusion is recommended here. In the following discussion below only the first three SPs are carried forward. However, it is recommended to perform TALTs at the four bias points, including Q2 in the search for a full set of signature parameters.

The next step is to estimate the amount of degradation in each signature parameter to give a 1 dB degradation in RF output power for the transistor or MMIC under consideration. This activity can be performed by observing large amounts of production data to obtain this relationship. Or it may come from simulations of the transistor or MMIC. For example, by observing large amounts of test data for a MMIC, the correlation might be established that a 10% reduction in I_{DSS} corresponds to a 1 dB reduction of P_{out}. Or by simulation of a MMIC, it might be established that a 25% reduction in transconductance g_{mpk} and a 700 mV positive shift of the threshold voltage V_T both (separately) correspond to a 1 dB change in P_{out}. These are the failure criteria for the signature parameters in this example. In general this must be found from data or simulations.

Having next performed two- or three-temperature DC-accelerated testing at these three Q-points, the Arrhenius plots for these signature parameters with the above failure criteria are shown in Figure 3-13a. No RF measurements are involved up to this point. Note that in the case of the low activation energy electron trapping case Q4, these degradations were extrapolated to the relatively long times shown. The mission temperature in this example is assumed to be 150 °C. Neither the Q3 nor Q4 test shows sufficient reliability for this mission.

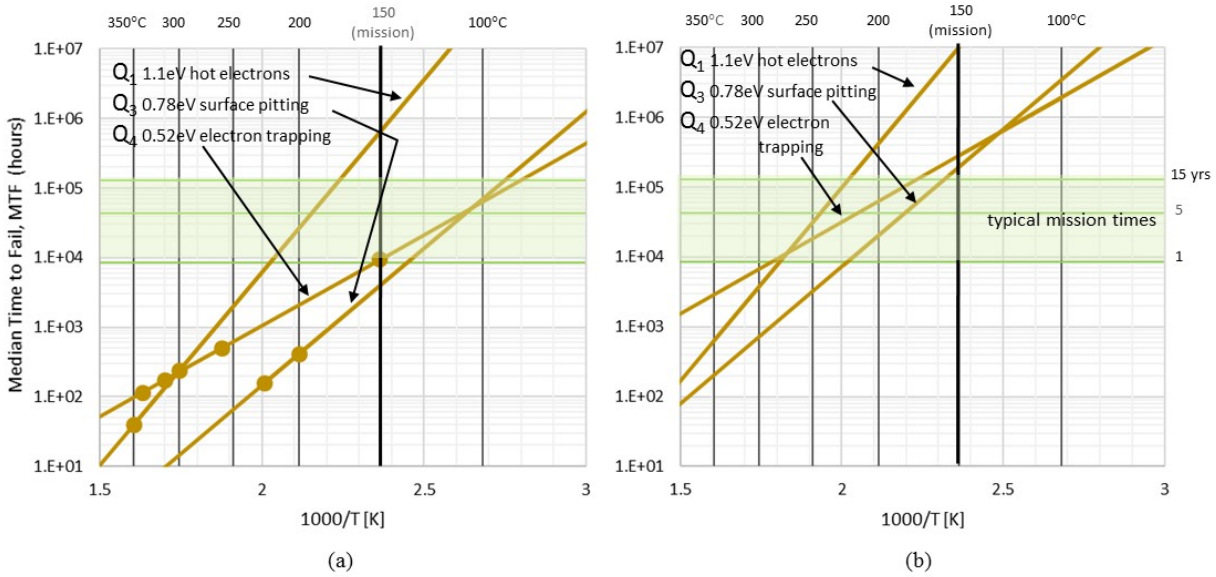


Figure 3-13. Arrhenius results (a) of DC tests for three example signature parameters and the translation (b) of these results to RF conditions using the method described herein.

However, the RF loadline might not access the Q3 or Q4 regimes very much during operation in the particular application. If so, the reliability might be considerably better in actual RF usage than is projected in Figure 3-13a. To ascertain this possibility, RF testing must be done. The RF test should be performed at the same power compression level as for the actual application and at an accelerated temperature that can give measurable degradations in laboratory times. Recommended RF lifetest channel temperatures are in the range of 200 °C to 350 °C. Here, in this example, the RF lifetest is performed at 250 °C. At various times, the RF test is interrupted, and DC measurements of the signature parameters are made. Figure 3-14 shows the results of the degradation measurements of the signature parameter Δg_{mpk} during the RF test as compared with those same degradations from the individual DC Q1-point tests. For this example, case the degradations are linear in $t^{1/2}$. It also might happen that the degradations are linear in time, logarithmic in time, or some other degradation form. This should be verified case by case. Figure 3-14 shows the average slope, a of Δg_{mpk} versus $t^{1/2}$ for the DC Q1 test translated to the RF lifetest temperature using its Arrhenius relationship. It also shows the RF lifetest degradations of the same parameter Δg_{mpk} versus $t^{1/2}$. Note that the RF degradation has a shallower slope, b. This is expected since the RF loadline passes through (or near) Q1 only for brief intervals per RF cycle. The ratio of the DC to RF slopes, a/b is 4. Using similar methods, the slope ratios for the DC Q3 and DC Q4 tests in this example are 7.1 and 5.5, respectively.

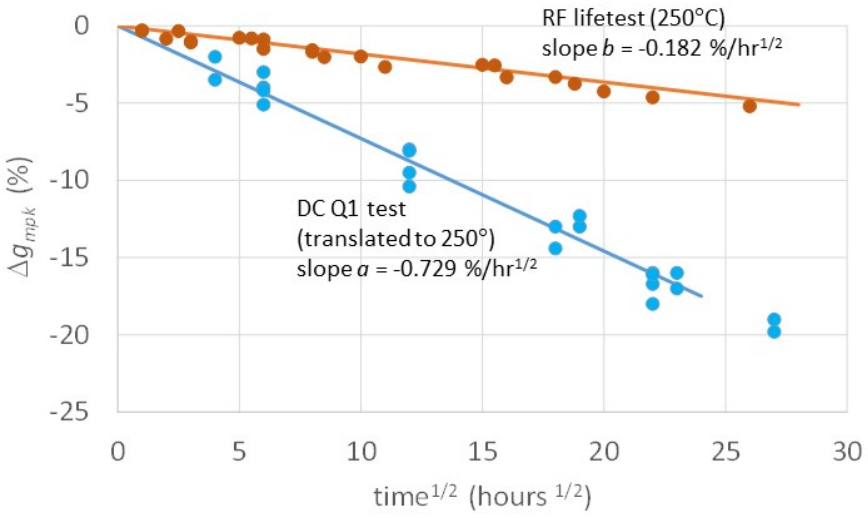


Figure 3-14. Degradations of the signature parameter g_{mpk} versus $t^{1/2}$ for the DC Q1 test and for an RF-driven lifetest.

Now that there is a relationship between the rates of degradation in $t^{1/2}$ between the RF and the DC signature parameters, it remains to translate these to MTF (median time to failure) values. The translation is given by

$$MTF_{RF} = \left(\frac{a}{b}\right)^2 MTF_{DC} \tag{3-5}$$

where the translation from known DC MTFs is made to the desired RF MTFs. The result of this translation is shown in Figure 3-13b for the three signature parameters chosen here. As can be seen, the three RF MTFs are now significantly higher than the original DC MTFs of Figure 3-13a. Using the signature parameter method, this example HEMT technology would be suitable for RF usage in a 10- or 15-year mission at 150 °C. The device will degrade at 150 °C mostly by the surface pitting mechanism in this example. However, at lower temperatures, such as at 100 °C, the electron-trapping mechanism will dominate the reliability.

The same approach may be used if the linearizations are chosen differently. For example, if degradations are found to be logarithmic in time (the degradation in percentage plotted versus $\log_{10}(t)$ is a straight line) with logarithmic slope a (% per decade) for the DC test, and b for the RF test, then the translation from DC to RF is given by

$$MTF_{RF} = (MTF_{DC})^{\frac{a}{b}} \tag{3-6}$$

Or if the linearization is found to be proportional to $t^{1/n}$, where n is a fitted value (the degradation in percentage plotted versus $t^{1/n}$ is a straight line), with slope a (%/hr$^{1/n}$) for the DC test and b for the RF test, then the translation from DC to RF is given by

$$MTF_{RF} = \left(\frac{a}{b}\right)^n MTF_{DC} \tag{3-7}$$

A number of assumptions have tacitly been made in the above description of the signature parameter qualification method. It is worthwhile to list them here:

1. The signature parameters are "pure"—that is, they reflect only the identified degradation mechanism.

2. The degradation mechanisms are independent—that is, one neither enhances nor prevents another.

3. The scaling factors such as $(a/b)^2$ are independent of temperature, allowing the RF lifetest to be run at any convenient temperature.

4. The RF lifetest represents actual usage.

5. The signature parameters do not saturate.

6. The degradation rates can be linearized (in this example as $t^{1/2}$).

These assumptions should be verified as part of the qual procedure. Note that in general, they require some level of proof. For example, the signature parameters may not actually be perfectly "pure" (assumption 1) or uncorrelated (assumption 2). A signature parameter such as I_{DSS} could possibly be affected by channel mobility, mobility in the drain access region, shifts in the threshold voltage, and changes in source/drain contact resistance. However, ascribing all the change observed to the one parameter (assuming it is pure) may actually be a worst-case assumption. This can be verified by separately assuming that each parameter has a different correlation to the RF degradation. The worst one (with the most correlation to RF degradation) could serve as a signature parameter.

For each signature parameter DC stress condition, it is recommended to devote a sample size of 20 (10 minimum) burned-in parts at two (minimum) or three temperatures at four Q-points for a total of $20 \times 3 \times 4 = 240$ (recommended) or $10 \times 2 \times 4 = 80$ (minimum) DUTs. Following the DC stressing, an RF lifetest with a recommended quantity of 20 (10 min) additional burned-in parts per each of three (two minimum) temperatures should be performed to establish the translations as described above. The RF DUT quantities are $20 \times 3 = 60$ (recommended) or $10 \times 2 = 20$ (minimum). If any failures occur, the exact causes should be determined using physical failure analysis techniques. The DUTs should be drawn from three lots of wafers. The total device quantity is 300 parts (100 minimum) assuming that four signature parameters are identified.

3.9 Failure Analysis

For any failures, especially catastrophic failures observed in the DC testing protocol described in Section 3.1 above, a failure analysis (FA) should be conducted. The FA planning should consider the following:

- High magnification optical inspection
- SEM (scanning electron microscopy)
- Mechanical cross sectioning
- FIB cross sectioning
- TEM (transmission electron microscopy) with imaging and chemical analysis
- EMMI (photon emission microscope) measurements
- IR imaging

Prior to any destructive failure analysis, judicious electrical testing is highly recommended. The origins of a degradation in s_{21} magnitude may arise differently. Electrical characterization is the key to determining

these causes. For example, s_{21} degradation could be caused by a trapped charge in the recess region, damage to the 2DEG conduction region, or to degradation of the source/drain ohmic contacts. More detailed electrical testing is one way to isolate these mechanisms. For example, trapped charges in the recess region are indicated by changes in the threshold or pinchoff voltages measurable by the transfer characteristics. The charge trapping can be observed under the high field biasing conditions with IR or EMMI imaging. Electroluminescence emanating from damage centers can be observed in many cases (Meneghini, 2011 and 2013; Hilton, 2016). Damage to the 2DEG is signaled by changes in the peak transconductance. Source/drain ohmic resistance changes can be detected from the common source IV curves at low drain voltage or R_{Don} measurements, while source/drain contact degradations can be detected by high-magnification optical microscopy or SEM images. Surface pitting near the gate can be observed in cross sectional SEM or TEM imaging and correlates to reduced drain current and transconductance. Many times a failure site occurs in small region along the width of a HEMT device, making its isolation for physical analysis difficult, especially if the site does not generate a hot spot or light. Often dramatic electrical changes are produced by relatively subtle physical manifestations. Figure 3-15 shows an example of a high-resolution TEM cross section showing a series of cracks and pits at both the drain- and source-edges of the gate of a HEMT with a gate length of 0.25 μm after being subjected to DC-accelerated stressing (Sin, 2011). It is recommended that physical analyses be performed to ascertain the failure modes observed during TALT or VALT.

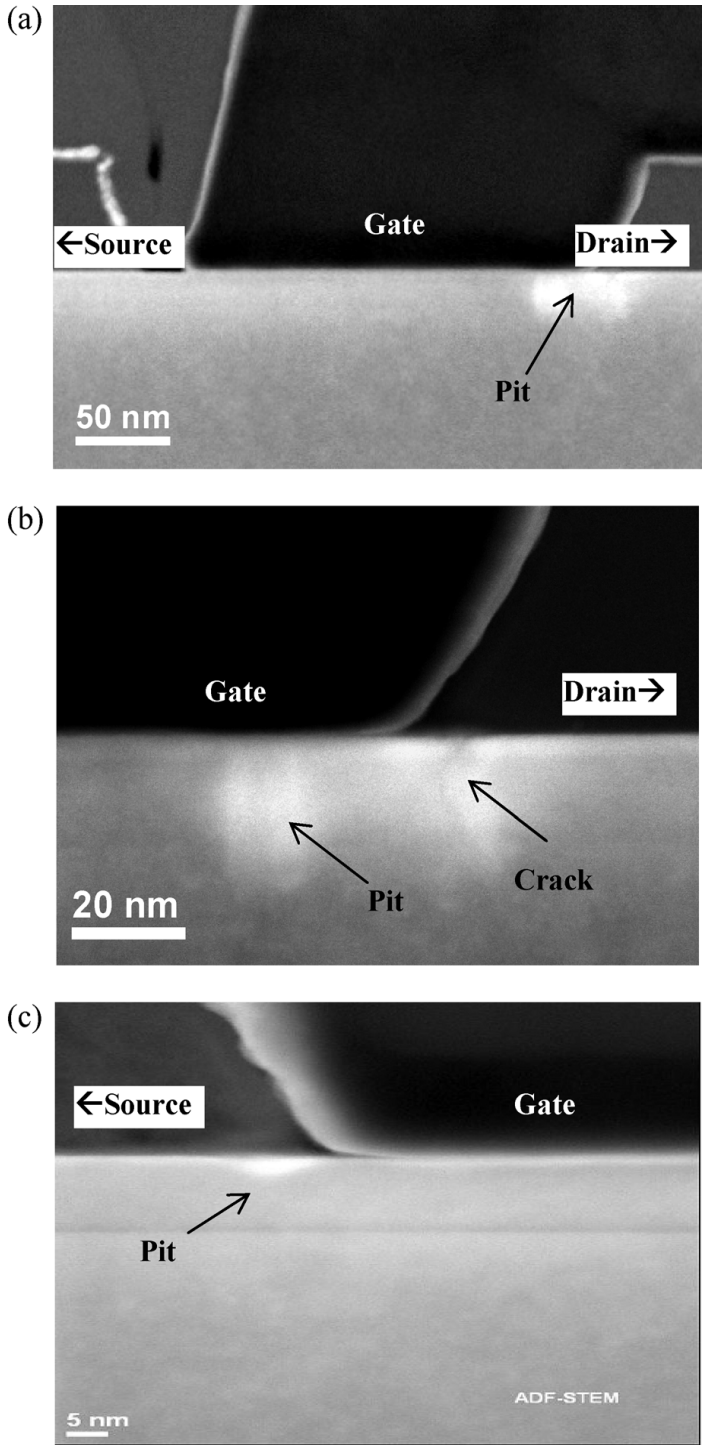


Figure 3-15. Cross-sectional high-resolution TEM images from post-stressed GaN HEMT samples. Pits and cracks are seen at the drain edge of the gate (a) with 150× magnification and (b) with 1M× magnification. At the source edge of the gate, a pit is also observed (c) with 1M× magnification. (Images graciously provided by Y. Sin and B. Foran, The Aerospace Corporation).

3.10 RF-Driven HEMT Accelerated Testing

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
10 min 20 nom	3	once	✓	✓		tailored for acceleration(s)

Although much more difficult than DC stressing, a large signal RF-driven lifetest should be performed as part of the qualification process. This is because DC stressing may accelerate some failure mechanisms differently (either more strongly or more weakly) than under more realistic RF usage. For example, depending upon the nature of the RF loadline, the surface pitting mechanism may occur reducing the drain current; hot electrons may be generated producing drain lag or drain current collapse; the Schottky gate may be affected changing the threshold voltage; the source/drain contacts may become more resistive due to high currents. At this time, it is not possible to recommend exactly how to electrically accelerate a correct mixture of failures with DC or pulsed testing that occur under actual RF-driven conditions. The following have been reported or suggested as modes of RF-driven acceleration:

- High levels of RF overdrive and/or compression
- Increased drain voltage below catastrophic breakdown
- Elevated temperature
- Temperature cycling to induce mechanical stress
- Pulsed operation inducing high peak temperatures and temperature gradients

A combination of all of these can be attained in an RF-driven lifetest.

An accepted reliability metric applicable to GaAs power HEMTs has been based upon the average gate current while under RF stress. So long as the overdrive is not sufficient to forward bias the HEMT Schottky gate during the RF positive peaks, the average gate current is an indicator of the hot electron density generated in the GaAs at the drain edge of the gate. A standard requirement is that this average gate current should not exceed 0.1mA/mm in GaAs HEMTs to prevent hot electron degradation. A similar metric does not exist in the GaN HEMT domain. Gate current, whether DC gate leakage or gate current when in RF operation, has not been found to correlate with GaN HEMT reliability.

Hot electrons produce damage of at least two types: (1) creation of defects at the gate-drain edge, and (2) trapping electrons in the access region causing increased drain resistance (Chini, 2011). Hot electron damage and charge trapping occur when the device loadline moves into the semi-on and off-state regions. Electroluminescence (EL) light is then generated by the hot electrons and can be sensed and correlated to damage and degradation (Meneghini, 2011 & 2013; Hilton, 2016). Measurement of electroluminescence is a laboratory technique that has not yet lent itself to routine reliability qualification, although it is an extremely useful FA technique. The hot electron damage mode is one of several that are possible during RF operation, particularly with high compression. It is important to perform an RF-driven lifetest in addition to the DC tests proposed previously.

The RF-driven lifetest should be tailored to the usage or application with as much acceleration as possible from each of these accelerants. Device loading should be similar to its anticipated usage as much as possible. It is recommended that at least one elevated temperature test be performed on a minimum of 10 devices. (A two-temperature RF-driven lifetest with 10 devices per temperature is highly recommended.) The temperature(s) should be selected to have sufficient acceleration to test for RF stress-induced degradation without inducing high-temperature failure mechanisms not seen in normal operation.

The RF drive should encompass the proposed usage of the device with as much overdrive as possible. If the anticipated usage of the HEMT is in a pulsed application, then a realistic pulse or signal waveform should be applied. Often an application will alternate from pulsed compression to uncompressed or small signal operation. If the anticipated usage is truly CW, then the actual drive level with some additional overdrive 1–4 dB above compression is recommended. Other general requirements are as follows:

- Frequent or continuous monitoring of the output power, DC input power (voltage and current) and baseplate or die mount temperature
- Realtime estimation of the channel temperature from the thermal resistance × dissipated power (dissipated power is DC input power less RF output power)
- Frequent or continuous adjustment of the RF input power so as to maintain a constant channel temperature despite possible reductions in RF output power as the device degrades
- Alternatively, frequent or continuous adjustment of the RF input power so as to maintain a constant RF output power, despite changes in channel temperature and power dissipation as the device degrades
- Periodic interruptions for cooldown to room temperature (or a selected measurement temperature) where the device electrical measurements outlined in Sections 3.5 and 3.6 are performed.

In performing this RF-driven lifetest, a realistic combination of device degradation mechanisms can be established. These should be compared with those observed during the DC stressing at the four bias conditions of Section 3.1. Where similar degradation mechanisms occur in comparing the DC to RF tests, Arrhenius parameters (activation energy and time scale factor) may be estimated. There will likely be a mixture of Arrhenius relationships for temperature at work along with electrical (current, voltage, or electric field) relationships such as power law, Eyring relationships, or others. These relationships should be separated and analyzed individually.

It also may be useful to perform RF-driven lifetesting on a test vehicle or MMIC that operates at a lower frequency than does the process or MMIC design capability. A lower-frequency RF-driven lifetest is often far less complex and may lend itself much more easily to the DUT quantities needed. Operation with a similar RF loadline, similar power output, similar dissipated power, and similar saturation level as the actual device of interest but at a lower frequency may be possible using a surrogate MMIC or HEMT designed or selected for the purpose. A load pull measurement may be needed to establish the correct test conditions.

3.10.1 Gate-Debiasing Effect

In the case where a GaN HEMT amplifier is to be operated in pulsed compression mode during RF-driven lifetesting, alternating with small signal operation, a caveat is in order here. Unless special attention has been paid to the gate-biasing circuit, adverse consequences may arise. Figure 3-16 shows a typical simplified MMIC gate-biasing scheme where the gate bias is separated from the RF source by means of a blocking capacitor. Inductors in the gate bias network present a high impedance for RF and maintain the DC level set by the gate bias source and resistor divider. The gate bias voltage is negative for Schottky diode-based RF and microwave GaN HEMTs and MMICs.

When a high-level RF input is present, the gate bias is disturbed. During compressed operation in the pulse, the gate becomes forward biased by Schottky gate diode rectification. The forward diode current

flows during the positive peaks of the RF signal, as shown by I_F in Figure 3-16. This current in turn charges the blocking capacitor with the polarity sense as shown. On each cycle the gate voltage V_G becomes more negative and will eventually reach equilibrium. When the pulsed compression ends, the gate is left with a much more negative bias than intended. A compliant bias network (with relatively high values of the biasing resistors R_1 and R_2) exacerbates the problem. When the pulsed compression ends, because the gate has been debiased, the amplifer gain may be very low. Eventually, the gate-biasing circuit will return the gate voltage to its intended value. But until this happens, a dropout of the amplifier output occurs. The problem is exacerbated further when a typical integrated circuit regulator (sometimes referred to as a low dropout regulator, or LDO) is used for the gate bias source. The LDO regulator is capable of providing only one "quadrant" of the current-voltage plane. In other words only negative voltage and negative current (in the direction of the arrow labeled I_B in Figure 3-16) are possible. What is needed to reset the gate bias is a current flowing in the opposite direction—a two-quadrant gate-biasing source is preferable. A two-quadrant source can sink or source current while the voltage is held fixed at the correct value.

To illustrate this point, Figure 3-17 shows some waveforms from a 20 W MMIC amplifier heavily compressed by about 10 dB during a 0.5 μsec RF pulse at a frequency of 1 GHz. When not being pulsed, the amplifier is input with a small signal CW signal, also at 1 GHz. The dropout after the pulse ends is evident in Figure 3-17a and lasts for several microseconds. The DC gate bias source is an integrated circuit one-quadrant regulator. Figure 3-17b shows the gate voltage V_G as it becomes debiased and recovers. The time constants for the recovery are dictated the blocking capacitance and the bias resistor R_2. The only source of positive current to restore the gate voltage comes primarily from resistor R_2. In some biasing schemes, R_2 is omitted entirely and there is no source of positive current. In that case the only source of restoring positive current comes from leakage, as shown in simplified form here by the R_{leak} resistance in Figure 3-16. In that case, depending upon the leakage, the recovery time may be exceedingly long, many milliseconds or longer. When the DC gate bias source is replaced with a two-quadrant voltage source, and both bias resistor values lowered by 10×, the same MMIC produces no dropout as shown by the output power waveform in Figure 3-17c. The bias network is made "stiffer" with lower resistances. A minor disadvantage of a stiffer bias network is its increased power dissipation. There is also a tradeoff between the recovery from compressed or overdrive pulse conditions and protection of the device. When the bias network is very compliant, the gate voltage quickly debiases and protects the device by tending to pinch off the channel, reducing dissipated power. The tradeoff is that the recovery time can be long (Colangeli, 2013).

It bears mentioning a caveat here: a dropout such as that seen in Figure 3-17a should not always be construed as being caused by trapping phenomena in a GaN HEMT or MMIC. It may be the result of the gate-biasing circuitry. In many cases the biasing circuit is internal to the MMIC amplifier, and it would not always be apparent whether pulse recovery is controlled by gate debiasing or by traps. Trapping phenomena and current collapse can certainly produce similar symptoms (Axelsson, 2016). In multistage amplifiers the individual stages may have separate bias networks or may share a single bias network. This complicates matters since successive stages may become compressed even if the first stage is uncompressed. Trapping-produced dropouts can be ameliorated using clever circuit techniques such as described by Tome (2019). Such techniques are effective if trap phenomena remain fixed throughout a mission. At this time, it is unknown whether the trapping phenomena will remain stable during a mission with aging, stress, radiation, etc. Nevertheless, it is very important to consider the biasing scheme when performing RF-driven lifetesting to assure that the device is operated in a manner similar to that in the mission.

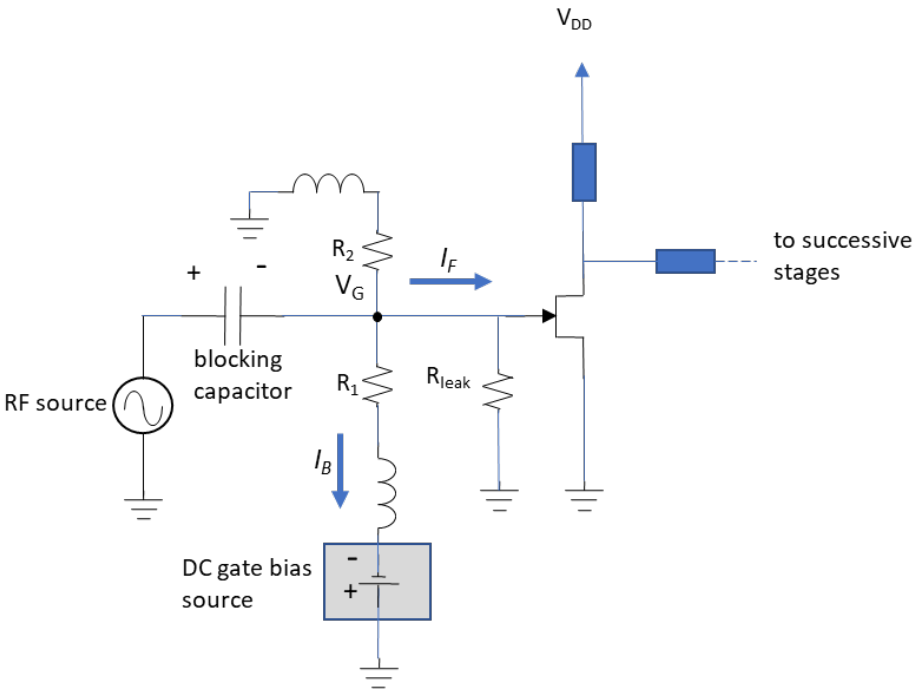


Figure 3-16. Typical simplified gate bias scheme. The gate can become debiased under high RF input drive.

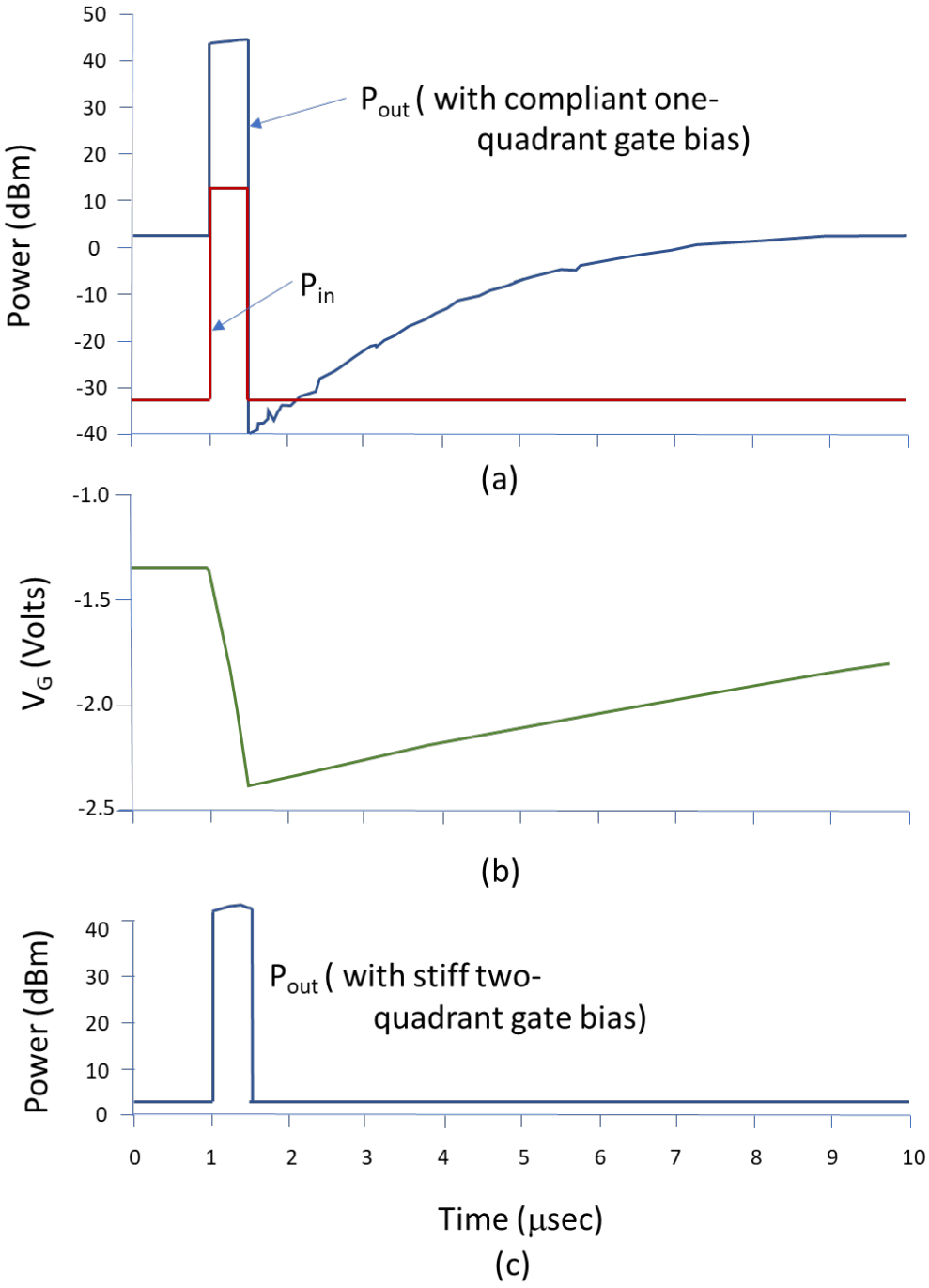


Figure 3-17. Waveforms illustrating the gate-debiasing effect. Output power from an amplifier showing (a) a dropout immediately after being pulsed into compression, (b) the gate voltage waveform indicating the debiasing versus time, and (c) the same amplifier output with a more effectual gate-biasing scheme.

3.11 HEMT Reliability Computation

In this section some example reliability computations are shown. The reliability metrics for HEMTs or other electronic devices employed in space programs are probabilistic statements such as:

- 25 FITs (failures in time) over 10 years with 90% confidence
- 0.2% failures in 15 years with 60% confidence

The first statement is that of an average failure rate over a certain time period (10 years). The second is a cumulative probability statement at the end of a time period (15 years). We assume here (and in fact the testing generally shows) that there is a wear-out phenomenon that limits the life of the device. Typical failure time probability distributions that are used for the wear-out of electronic components are the lognormal distribution and the Weibull distribution. Usually, a statistical analysis assuming the lognormal-Arrhenius assumption such as that described in JEDEC standard JEP118A is used for each individual failure mode. A Weibull failure distribution as an alternative to the lognormal may provide a better match to the failure data. In the following, some typical reliability computations are provided as a point of reference.

For a wearout phenomenon in a GaN device having a typical lognormal failure distribution with a shape factor $\sigma = 0.7$ and a median time to fail $t_{50} = 10^6$ hours, for example, an estimate of the probability of device failure by the end of a mission time of $t_m = 15$ years (1.31×10^5 hours) is obtained using the lognormal cumulative distribution function

$$P_f\left(t_m\right) = \Phi\left(\frac{\ln t_m - \ln t_{50}}{\sigma}\right) = 0.19\% \tag{3-8}$$

where Φ is the standard normal cumulative probability distribution. An approximation to the lower confidence limit of the median time to fail for a lognormal distribution is

$$t_{50.LCL} = \exp\left(\ln t_{50} + \sigma \frac{T_{N-1,1-C}}{\sqrt{N}}\right) \tag{3-9}$$

where C is the confidence factor (for example $C = 0.9$ for 90% confidence), N is the sample size used to develop the modeled median time to failure t_{50}, and $T_{N-1,1-C}$ is the lower tail of Student's T-statistic with N–1 degrees of freedom, and fractile 1–C. Note that $T_{N-1,1-C}$ is a negative quantity for a lower confidence limit. For example, for a sample size of $N = 70$ devices, and confidence factor $C = 0.9$, the T-statistic is $T_{69,0.1} = -1.294$, and the lower confidence limit for the median time to fail is $t_{50.LCL} = 8.97 \times 10^5$ hours. The upper 90% confidence limit of the probability of failure by the end of a 15-year mission is

$$P_{f.UCL}\left(t_m\right) = \Phi\left(\frac{\ln t_m - \ln t_{50.LCL}}{\sigma}\right) = 0.30\% \tag{3-10}$$

Note that a lower confidence limit on the median time to fail leads to an upper confidence limit on the probability of failure.

Alternatively, a Weibull distribution may better fit the failure time distribution. For a two-parameter Weibull distribution, the relationship between the median time to fail t_{50} and the Weibull characteristic life α is

$$\alpha = \frac{t_{50}}{\left(\ln 2\right)^{1/\beta}} \tag{3-11}$$

where β is the Weibull shape factor. The Weibull characteristic life occurs at the time t_{63} where $1 - \exp(-1) = 0.632$, or 63% of the population fails. With a median time to fail of $t_{50} = 10^6$ hours and a typical Weibull shape factor of $\beta = 3$, an estimate of the probability of failure at the end of a 15-year mission is found from the Weibull cumulative distribution function

$$P_f = 1 - \exp\left[-\left(\frac{t_m}{\alpha}\right)^{\beta}\right] = 0.16\% \tag{3-12}$$

An approximation to the lower confidence limit of the Weibull characteristic life is

$$\alpha_{LCL} = \left[\frac{N t_{50}^{\beta}}{\chi^2_{N+2,1-C}}\right]^{1/\beta} \tag{3-13}$$

where $\chi^2_{N+2,1-C}$ is the chi-square distribution with $N+2$ degrees of freedom and fractile $1-C$. For example with a sample size of $N = 70$ devices and confidence factor $C = 0.9$, the chi-square statistic is $\chi^2_{72,0.1} = 87.7$, and the lower confidence limit on the characteristic life is $\alpha_{LCL} = 9.28 \times 10^5$ hours. The upper 90% confidence limit of the probability of failure by the end of a 15-year mission is

$$P_{f.UCL} = 1 - \exp\left[-\left(\frac{t_m}{\alpha_{LCL}}\right)^{\beta}\right] = 0.28\% \tag{3-14}$$

Finally, an upper 90% confidence limit on the average failure rate (AFR) during its mission is

$$\text{AFR} = \frac{-\ln\left[1 - P_{f.UCL}\right]}{t_m} \times 10^9 \tag{3-15}$$

The AFR is a way to represent the increasing wearout failure rate (whether a lognormal or Weibull failure time distribution) by a constant failure rate averaged over the mission time. When mission time t_m is expressed in hours, the AFR is expressed in FITs. The upper 90% confidence of AFR over 15 years is 22.9 FITs and 21.5 FITs for the above example lognormal and Weibull assumptions, respectively. Note that for a wearout distribution, the bulk of the device failure propensity occurs late in the mission.

The instantaneous failure rate (also called the hazard rate, Trindade, 2012) increases with time as wearout proceeds. The instantaneous failure rates at the end of the 15-year mission with 90% confidence are 99.7FITs and 64.5 FITs, respectively, for the lognormal and Weibull examples here. These are much higher than the AFRs. This simply means that by the end of the mission, the likelihood of failure is increasing rapidly in the device. The dissimilarity between these instantaneous failure rates lies in the different shapes of the two distributions.

Note that in these approximations for obtaining confidence limits, some liberties were taken. It was assumed that the shape factors are known exactly and that the variability lies only in the median or characteristic times. This is not always the best approximation, but the results can always be checked for sensitivity by varying the shape factors. Also not included is the (sometimes large) extrapolation risk incurred when short accelerated times are projected to much longer usage times. A more rigorous analysis of lifetest data can be made by performing a regression analysis (Scarpulla, 2000) maximum likelihood analysis (NIST, 2012) or by using bootstrap methods (Efron, 1998).

Also worth mentioning is that in Section 3.2, time-to-fail models are postulated to have voltage dependencies taking various forms. A recommended specification of maximum safe operating voltage $V_{DSmax.safe}$ is discussed in Section 2 and in Appendix D. This maximum safe voltage specification is recommended to be paired with a specified reliability with a certain confidence level. This is actually a reliability-based specification that can be verified analytically. The median time to fail t_{50} at the given $V_{DSmax.safe}$ should be computed from the selected model, and the associated reliability with the specified confidence determined as above. As for selecting an appropriate value of $V_{DSmax.safe}$ for a particular mission (other than a typical one), a separate calculation is needed. See Appendix H for specific recommendations.

Besides the HEMTs themselves, it is necessary to compute similar reliability metrics in a MMIC for the MIMCAPs, TFRs, conductors (electromigration reliability), etc. The overall MMIC represents a series system for reliability prediction purposes consisting of n_1 HEMTs, n_2 MIMCAPs, n_3 TFRs, n_4 conductors, etc. All the individual AFRs may be added (assuming failure rates are constant) for a series system in order to obtain the overall MMICs reliability. More complex reliability models that take into account the actual failure probability distributions may be more appropriate.

3.12 Long-Term Test or "Test-Like-You-Fly"

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
30	3	once	✓	✓		simulating 15% of mission, min.

The final proof of the reliability of HEMT operation is to perform a "test like you fly" (TLYF) test. This test should be conducted under realistic RF usage conditions with device loading as similar to its anticipated usage as much as possible. The test considerations should be similar to those for the RF-driven lifetest as described in Section 3.10. However, there should be no acceleration or only mild acceleration. For example, the channel temperature should be similar to that anticipated under usage conditions. The test should be conducted for a long duration—at least 15%—of the anticipated usage or mission time. For example, for a 10-year mission, a minimum 1.5-year-duration test is recommended. Because of the relatively long duration, it is recommended that this test be begun in the development phase.

A minimum device quantity of 10 devices each from 3 wafer lots is recommended. The purpose of this test is to eliminate the possibility of any hidden or "sneak" failure mechanisms, not necessarily accelerated by temperature. It is important to ensure that unanticipated low activation energy mechanisms are not present in long-duration applications. This test should include periodic measurements of RF and DC parameters, using the measurement types listed in Sections 3.5 and 3.6 as a general guide. The actual performance parameters of the device under test are most appropriate for consideration for a TLYF test. An example of a small quantity TLYF test on GaN MMICs may be found in Scarpulla (2019).

The TLYF tests should be conducted with the same packaging environment as the final configuration. For hermetic applications, the DUTs should be packaged in an identical package with identical sealing gas as for flight if possible. Alternatively, devices to be hermetically sealed may be subjected to TLYF testing with a purge gas identical to the intended sealing gas, typically dry N_2. For nonhermetic applications, it is recommended to perform TLYF tests with the actual PEM package, with identical molding compound, wirebonds, lead frame, etc. In cases where this is not feasible, devices intended for nonhermetic usage should be tested in laboratory air.

3.13 Considerations for GaN HEMT-based MMICs

In a particular GaN HEMT-based MMIC, the active devices may not be fully accessible, being embedded in the circuitry. For this reason, some of the HEMT device level tests described in the preceding paragraphs may not be feasible. It is highly recommended that test structures consisting of individual HEMTs be fabricated especially for reliability evaluations needed for qualification. The HEMTs should be similar in size and function to those in the final product device.

Product-level MMICs are well suited as test vehicles for RF-driven lifetests (Section 3.10) and TLYF tests (Section 3.12). MMICs are ideal test vehicles since the actual HEMT loading and circuit environment is well defined. However, it may not be practical to require extensive testing of a large variety of MMICs of similar design principles, differing in performance attributes. A fabrication line is capable of many different MMIC types, with different bandwidths, operating frequencies, power levels, etc. Of the many product MMICs that may be available, the qualification organization when necessary should define one or a few circuits (commonly called "standard evaluation circuits," or SECs) that serve as representations of the product line. Criteria for selection of an SEC are described in the IC military standard MIL-PRF-38535 para. H.3.4.3 (2013). The goal is that the HEMTs and other structures on the SEC are the basic building devices and represent the MMICs to be flown.

3.14 Qualification for Electromigration

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
90 per layer	3	once	✓	✓	✓	30 DUTs per temperature per metal layer

The current densities in metal conductors (typically Au metallization is used in GaN HEMT technologies) must be kept under control in order to avoid the electromigration effect. Electromigration is the mass transfer of metal ions under the influence of the "electron wind" in a current-carrying conductor. Electromigration can lead to open circuits (at the cathode end) and shorts or hillocks (at the anode end) of a metal line. Test methods and test structures are discussed in detail in JEDEC specification JESD202 para. 2.3 (2006). It is recommended to adopt the test structures as described therein even though they were originally intended for Al and Cu lines in more conventional Si-based technologies. In GaN HEMT technology, electroplated Au is the preferred metallization, and Au electromigration test structures as described in Kilgore (2005) serve this purpose equally well. The IC military standard MIL-PRF-38535L para. A.3.5.5 (2013) specifies a maximum current density of 6×10^5 A/cm^2 for Au. However, it must be pointed out that this military standard was developed in the Si era when the maximum metallization temperature was kept well below 125 °C. For GaN HEMT technologies, the temperatures may be considerably higher than this.

It is recommended that rather than using an older current density guideline, the electromigration failure mode in any GaN technology be characterized fully for space qualification. To illustrate the danger of using a simple guideline, consider the following. A fairly typical accelerated Au electromigration experiment from Kilgore (2005) gave an MTF of 148 hours with a current density of 2 MA/cm^2 at 372 °C. The Black's equation parameters also taken from Kilgore were $n = 2$, $E_A = 0.6$ eV and a lognormal shape factor $\sigma = 0.7$. Using these values at 125 °C and at the current density of 6×10^5 A/cm^2 (per the MIL-PRF guideline), a Au conductor in a 15-year mission will experience an AFR of 3.5 FITs. This would be acceptable in many applications. However, raising the temperature to 175 °C as might be required in a GaN HEMT power application elevates the AFR to 2700 FITs. This is quite undesirable. It happens because of the rapidly increasing wearout failure rate of a lognormal time to failure distribution. Utilizing the existing Au electromigration standard current density for GaN may well be unacceptable. Therefore, it is recommended here to properly characterize electromigration in Au metallization processes for space qualification rather than to utilize existing older standards that may not always be applicable. From this characterization, a much-reduced maximum allowable current density for GaN devices emerges.

Gate metallization is sufficiently different from standard metal layers to warrant special attention. Gates are often defined by electron beam lithography, and the HEMT gate fingers are much finer than standard metallization layers. Au gates are commonly used, but other metals are common, too, such as Mo, W, TiN and other refractory metals, or base metals such as Ni or Al. Many gates are composed of stacked metal layers. The MIL-PRF-38535 provides maximum current density guidance for some metals in Si technologies, but gate lines should be approached with caution for the reasons stated above for Au. Furthermore, the gate electrode (typically at the gate feed) is often the point of highest current density, especially if compression occurs that drives forward gate current during the RF cycle. This condition is quite different than in a standard metal line. A combination of measurements and modeling is recommended to ascertain the current density (amps/cm^2) at this point under these conditions. Special gate line test structures such as end-to-end gate stripes are recommended for electromigration testing. Gate metal may also migrate under the influence of mechanical strain induced by thermal coefficient of expansion mismatches or by as-processed internal stress. At elevated temperature or accompanied by a thermal gradient in powered operation, gate metal may self-diffuse and cause open failures (Paine, 2017). For this reason, gate metallization deserves special scrutiny.

It is recommended that 30 samples at a minimum be tested for each of three temperatures per metal layer (including the gate finger as a distinct layer) according to the JESD202 standard, and that the samples be drawn from three lots or wafers. Therefore, for each metal layer, a complete electromigration study requires 90 test structure samples.

3.15 Qualification of Thin Film Resistors

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
5 step-stresed, 90 for TALT	3	once	✓	✓	✓	• follow 4-step process (see text) • TFR test structures recommended

Thin film resistors (TFRs) in GaN HEMT MMIC technologies are formed by sputter deposition or ALD (atomic layer deposition) of a metal film followed by patterning of the films. The films are typically 20 to 50 nm in thickness, are composed of NiCr, TaN, or TiW, and have sheet resistances of 50 to 200 Ω/☐.

More recently, high-resistivity films of TiWSi have been employed with sheet resistances of a few thousand Ω/□. The resistors are deposited upon and passivated with dielectric layers such as Si_3N_4 or SiO_2. Under long-term stressing with current density and temperature, three failure modes appear in these films:

- phase changes in the metal film
- oxidation of the metal film
- interdiffusion/electromigration of the electrode metal and the metal film

If the resistor is subjected to a sufficiently high temperature because of the combination of its internal joule heating and externally applied temperature, these failure modes begin to ensue. The resistor then may change in value, and failure is determined by a certain fractional resistance change. It is not always apparent whether aging of resistors might cause a gradual increase (Lee, 2004; Baca, 2017) or a decrease (Drandova, 2010) in the resistance. Eventually, thin film resistors tend to catastrophically fail "open." A "critical current" may be defined (Baca, 2017) as the maximum instantaneous current that the resistor can tolerate without a permanent change in its resistance value. A "critical temperature" (or power density) at which the resistor deviates in value by a certain amount beyond its TCR (thermal coefficient of resistance) (Bansal, 2016) can also be defined. Both these critical quantities are extremely geometry dependent. A large, square resistor may have a higher temperature at its hottest point (center) than a small square resistor of equal resistance value when the same power density (power per unit area) is applied. Similarly, a short, wide resistor may have a higher critical current density than a long, narrow resistor of the same area. The variation in critical current density or power density among various geometries can exceed 10×. A characterization of these geometry and thermal factors is necessary across the design space of thin film resistors as part of a process qualification for space usage. The operation of the resistors at the highest anticipated power dissipation and ambient temperature should never approach the critical current or temperature for the particular geometry. The resistance change due to aging or degradation must remain within tolerable bounds.

It is recommended that a four-step procedure be employed for space qualification of TFRs:

- A modeling effort should be conducted to provide designers with a guideline for sizing of resistors. The guideline should take into account the thermal resistance and temperature rise of a resistor as a function of geometry and power density (power per unit resistor area) or current density (current per unit resistor width). A simple guideline such as a maximum current density of 0.5mA/μm might be satisfactory. A more sophisticated guideline taking account of varying thermal resistances and power densities as functions of geometry could also be advantageous to enhance performance.

- A verification of the temperature rise and thermal resistance model should be carried out. The temperature rise should be measured using an IR microscope or a liquid crystal coating on a resistor selected from the design space guideline (see Appendix E of this document for guidelines on the measurement of temperature).

- A power or current step stress at the maximum anticipated die temperature should be performed from a resistor selected from the design space guideline. The power or current at which the resistor begins to change its value is an indicator of the temperature rise at which reliability testing should be performed. Failure criteria depend upon applications; however, a 1% resistance change is recommended as a default failure criterion. It is recommended to utilize power or current steps 12 to 24 hours in duration. It is recommended to utilize a sample size of 5 DUTs for the step stress.

- Based upon the step stress results, a three (or more)-temperature lifetest should be performed at selected temperatures, selected temperature rises or selected power densities (see Lee, 2004 and Baca, 2017) for examples of multi-temperature TFR lifetests). The lifetests should be performed on a resistor chosen from the design space, preferably one with a high thermal resistance, such as large square resistor. Separate tests on various resistor geometries are also recommended. The results of the lifetesting should be used to predict the resistor reliability. It is recommended that at least 30 samples be stressed per temperature. Therefore, a three-temperature lifetest (3TLT) requires 3 × 30 = 90 samples per resistor geometrical size.

Note that in space usage, with vacuum or in a hermetic package, oxidation of the metal as a failure mode might be eliminated. It is worthwhile, however, to point out that the surrounding passivating layers of the metal film may contain oxygen or water and that oxidation of the metal might still occur. Nonetheless, for space qualification, performing the accelerated tests in dry N_2 is preferable.

3.16 Qualification of Bulk Resistors

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
5 step-stresed, 90 for TALT	3	once	✓	✓	✓	• follow 4-step process (see text) • bulk resistor test structures recommended

Bulk resistors are implemented in some GaN MMIC technologies. The resistor is formed by utilizing the bulk GaN layer, with the AlGaN layer removed, eliminating the 2DEG. The resistance value is then determined by the bulk GaN film, typically 10–200Ω/□. Ohmic contacts usually employ the same metallization and annealing steps as those for the HEMTs themselves in the MMIC process. The current density in these contacts is often like those in a HEMT, especially for short-length resistors. In some cases, the self-heating in the bulk resistors can be substantial, leading to high-temperature operation. There have been no reliability studies of GaN bulk resistors to date; however, in earlier GaAs technology, bulk resistors have been subjected to accelerated testing for reliability (Sabin, 2000a & b). The failure mechanism in the GaAs bulk resistors was found to be catastrophic once very high temperatures were achieved through self-heating. The catastrophic failures are a result of the Ni diffusion barrier becoming less effective at high temperatures, allowing the diffusion of Au into the GaAs, then resulting in a sudden filament. For lower, more realistic temperatures, the failure mechanism in GaAs bulk resistors is believed to be a gradual loss of electrical contact between metal and semiconductor. In the studies referenced (Sabin), the resistor value always increased with aging when noncatastrophic. Depending upon their construction, similar effects may occur in GaN bulk resistors. The GaN bulk resistor ohmic contacts may have similar failure modes as for the very similar ohmic contacts for the HEMTs (Wua, 2014; Piazza, 2009). However, geometries and materials are different, especially since the bulk resistor don't have the 2DEG.

For GaN bulk resistors it is recommended that the same four step procedure be used as recommended in Section 3.15 for TFRs. The same quantity of 90 DUTs is recommended for 3TLTs, with the tests performed in dry N_2. A preceding step-stress test, stepping the current or voltage is recommended with a quantity of 5 DUTs. However, a 10% change in resistance is recommended as a failure criterion for bulk resistors, unlike TFRs.

4. Qualification for Environmental Factors

The following paragraphs list some of the environmental factors (other than temperature and electrical bias) that should be considered when qualifying a GaN HEMT device or process.

4.1 Air Sensitivity

Many high-reliability space applications have strict requirements for hermeticity if only as a protectant from harsh handling conditions or particulate contamination. In other cases, hermeticity is required at a lower level of assembly to permit plasma or solvent cleaning at higher assembly levels. In some cases, however, nonhermetic applications may be warranted.

It is recommended that the anticipated environment (hermetic vs. nonhermetic) be assessed and the GaN HEMT technology be qualified in that environment. For hermetic packages usually sealed with N_2, Ar, He, or mixtures, it is recommended that all testing as described in Section 3 be performed in systems purged with dry N_2. If nonhermetic applications are to be qualified, then the tests should be performed in laboratory air with relative humidity controlled to be within the range 30% to 70%.

4.2 Moisture Sensitivity

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
30	3	once		✓		open package

In nonhermetic applications, it is always a possibility that there will be moisture accumulation. High-humidity environments may occur. If a payload is launched under high-humidity, warm-weather conditions and reaches enough altitude, the temperature drops precipitously to subzero levels, and any moisture trapped in the nonhermetic package will condense or freeze. For this reason, it is recommended that moisture sensitivity testing be performed on any GaN device or process that is to be qualified for a high-reliability, nonhermetic application. One proposed failure mechanism induced by moisture (Gao, 2014) is an electrochemical reaction at the "foot" of the gate metal. Under bias, temperature, and humidity, erosion or pitting of the GaN or AlGaN cap layer occurs, resulting in failures. The pitting results in a permanent decrease in drain current and also an increase in the drain current collapse ratio (observed with PIV testing). One suggested mechanism to explain this is that the pits decrease the average thickness of the AlGaN barrier and thus decreases the average electron concentration in the channel. This leads to a higher access resistance and subsequently a lower drain current. It has also been suggested that this corrosion mechanism rather than the so-called inverse piezoelectric effect (IPE) is the root cause of pits, as tests are often performed in air that contains some moisture. If the tests are performed in dry N_2, this corrosion mechanism might not appear. More work remains to be done to answer these questions.

It should be noted that while performing elevated temperature lifetests, normal laboratory air (relative humidity 30–70%) becomes dry air with exceedingly low relative humidity. Moisture-related failure modes are therefore not activated. For this reason, it is recommended that a DC stress test at the Q3 operating point (low current and high voltage) as described in Section 3.1 be repeated under 85/85 conditions (85 °C and 85% relative humidity) under bias. It is recommended that this test be performed for 1000 hours with periodic room temperature device characterizations every 250 hours per Section 3.1. A device quantity of 30 drawn from three lots or wafers is recommended with zero failures after the test completion. It should be recognized that the typical THB (temperature humidity bias) test on

plastic-encapsulated microcircuits (PEM) is similar in nature. However, its purpose is to ascertain whether the device (usually a silicon semiconductor die) is affected by moisture incursion through the plastic or if there are other problems, such as moisture-induced delamination of plastic encapsulant, known as the "popcorn effect." Here we are interested only in the moisture sensitivity of the GaN die itself and its passivation.

4.2.1 Moisture, Ammonia, and GaN Devices in a Hermetic Package

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
6	3	once	✓			• Perform 320 hr. bake • perform RGA test for NH_3

Traditional military standards require that hermetic packages and modules contain an internal water vapor content of no more than 5,000 ppmV. These standards are

- MIL-STD-883K,
  - Method 5005.17 Qualification and Quality Conformance Procedures
  - Method 5010.4 Test Procedures for Complex Monolithic Microcircuits
- MIL-PRF-38543J
  - Appendix C Generic Performance Verifications for Hybrid and Multichip Module Technologies, para. C.7.5.4.9 Internal Water Vapor.

RGA (residual gas analysis), otherwise called IGA (internal gas analysis), is the test method used to measure water vapor in hermetic packages per:

- MIL-STD-883K,
  - Method 1018.10 Internal Gas Analysis
- MIL-STD-750E,
  - Method 1018.6 Internal Gas Analysis

These existing standards for the maximum moisture level permissible and test methods for their determination have served well the hybrids and hermetic packages used with Si or GaAs devices. The primary concern has been with moisture generating corrosion in metals, or producing layers of liquid water below the dew point. These concerns certainly exist for GaN HEMT devices as well. However, GaN has some new properties that have not been considered to date. GaN itself can react with water and produce ammonia, according the chemical reaction

$$2GaN + 3H_2O \rightarrow Ga_2O_3 + 2NH_3$$

Gallium oxide is created at the surface of the GaN, and ammonia is liberated. The reaction is activated with electrical bias, UV light (Seo, 2002) and likely ionizing radiation. In a long space mission with a GaN device mounted in a hermetic package containing up to 5,000 ppmV of water vapor, there is some possibility that ammonia in vapor phase may be generated. It is unknown currently whether the existing 5,000 ppmV moisture level is compatible with the use of a GaN HEMT device. The buildup of ammonia inside a microwave housing or hermetic package could create many problems, such as corrosion of any other materials, such as metals like Al, Kovar, or others. These materials may reside inside the package or hybrid along with a GaN die. Ammonia may be capable of penetration through polymeric coatings or internal seals. It may cause poisoning of passive devices.

It is recommended that all proposed GaN devices in hermetic package be investigated using RGA after temperature exposure while under bias. Ammonia levels should specifically be gauged. If elevated levels of ammonia are observed, the other contents of the package should be carefully evaluated for ammonia sensitivity, corrosion, or ammonia poisoning. Judging from the chemical reaction posed above, 5,000 ppmV of water vapor if fully hydrolyzed would create 3,333 ppmV of ammonia vapor. It is unknown whether this level is harmful to the HEMT or other devices inside a microwave hybrid or module.

The GaN device may itself be sensitive to ammonia. For example, the region between the gate and drain might have a sensitivity to ammonia generated elsewhere on the die. Unpassivated chip edges may be capable of generating ammonia. Not enough is known about the levels that can be generated or the sensitivities of the GaN devices to recommend any guidelines at this time. It is recommended, however, that tests be conducted to ascertain the ammonia sensitivity of a GaN device that is intended for hermetic packaging in a space mission. Tests with various levels of ammonia in nitrogen carrier gas would be needed. Tests that include ionizing radiation are recommended since this may activate the reaction that produces ammonia.

Similar reactions can occur in high-temperature nitride packaging materials and substrates now being proposed for use with GaN devices, such as AlN. The reaction is

$$AlN + 3H_2O \rightarrow Al(OH)_3 + NH_3$$

Aluminum hydroxide (a whitish solid at room temperature) is produced along with ammonia. It is recommended that nitride-based hermetic packages or substrates proposed for use with GaN devices be carefully investigated. After exposing a sealed hermetic package to elevated temperature with realistic internal moisture levels, RGA tests are recommended to determine the internal levels of ammonia, hydroxides, and other possible reaction products with the moisture. It is recommended that users first bake flightlike hermetic packages containing GaN devices at 150 °C for 320 hours prior to RGA testing. A DUT quantity of 6 packages from 3 three lots is recommended.

4.3 Water Droplet Test

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
6	3	once		✓	✓	open package or die

For similar reasons as described in the preceding section, it is recommended that water droplet testing be performed on any GaN device or process that is to be qualified for a high-reliability, nonhermetic application where condensing moisture could be a possibility. Some HEMT processes incorporate polymeric coatings such as Parylene™ (polyxylylene) or BCB (benzocycobutene) intended to repel moisture.

The test should be conducted with the HEMT device in the “off” condition with the channel pinched off and the drain voltage at the maximum usage value. For a MMIC, the same condition should be used. The test is conducted by applying a water droplet atop the active area of the HEMT. The device must survive for 5 minutes. A sample size of five devices drawn from three lots or wafers is recommended. An open package or a probed die are suitable test vehicles.

4.4 Hydrogen Sensitivity Test

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
12	3	once		✓		open package

RF and microwave housings are usually internally electroplated with Ni followed by Au, both containing trapped hydrogen. Kovar bars from which the housings are machined are usually annealed in forming gas, consisting of approximately 5% hydrogen. Also, certain microwave absorber materials also can contain hydrogen. Therefore, over time the internal cavity of a sealed housing may begin to contain small amounts of H_2 gas as outdiffusion from these sources occurs. Hydrogen concentrations up to 15,000 ppmV (1.5% by volume of internal sealing gas) have been typically observed. Even higher numbers have been reported occasionally. Unfortunately, this causes a hydrogen poisoning problem in GaAs HEMTs. The gate metal is typically Ti/Pt/Au (bottom to top) in first-generation GaAs HEMTs. A reaction of the H_2 with the Ti occurs to create TiH_x with the Pt layer as a catalyst. The volume change as Ti is converted to TiH_x is responsible for a piezoelectric stress, which develops a charge, causes a threshold shift, and changes the device characteristics. Also, the Schottky barrier height of the gate is modified, further changing the characteristics. These changes occur slowly, are thermally activated and concentration dependent, but can ultimately lead to failure. In a space environment, no microwave housing is perfectly sealed, so theoretically, the excess hydrogen along with the sealing gas will be eventually evacuated. Unfortunately, this is not a guarantee, and the hydrogen poisoning can occur long before full evacuation via package leaks.

This problem was largely mitigated using hydrogen getters in the packages, or by less sensitive, alternative gate metals. Hydrogen sensitivity is usually associated with hermetic microwave packages for this reason. Nonhermetic environments with high hydrogen concentrations are also a concern.

For GaN, which is even more highly piezoelectric than GaAs, this effect has been reported in one instance for a GaN microwave device (He, 2019). In addition, sensitive GaN hydrogen detectors with Schottky gates, especially containing Pt or Pd as a catalyst layer, are widely reported (Song, 2005). Therefore, it appears to be prudent to assess the hydrogen sensitivity of any GaN technology that may be utilized within a microwave housing. The usual test is to perform an exposure in forming gas and determine the magnitude of any electrically observed changes.

The changes typical of GaAs technologies are expected be similar in GaN devices. Characteristic changes and failure conditions are as follows:

- reduction of transconductance at given bias conditions Δg_m of 10%
- change in the drain current for specific bias, or changes in ΔI_{DSS} greater than 10%
- change in the threshold voltage ($|\Delta V_T| > 50$ mV)
- other failure criteria per Section 3.7

It is recommended to expose a sample of 12 devices drawn from three lots or wafers in forming gas (5% H_2 in dry N_2) for 1,000 hours at 250 °C with measurements taken before and after the exposures. Changes in characteristics within these values are considered acceptable. The devices may be passive (unbiased) during the forming of the gas exposures. The device would then be qualified for use in Ni/Au plated or Kovar housings without the need for a getter.

4.4.1 Hydrogen Mitigation

Should the GaN technology prove to have a hydrogen sensitivity, a number of steps can be carried out. Also, options are available to control the hydrogen content inside a hermetic microwave package. These are listed here as follows:

- **Package Bake-out.** Some success has been achieved by performing a bake-out of the primary hydrogen sources (package and lid) to varying degrees of success. The effectiveness is highly dependent on temperature and duration and varies significantly from manufacturer to manufacturer and to a lesser degree from lot to lot. The most effective method is to bake at 350 °C for 48 hours in a vacuum that is routinely evacuated or with dry N_2 flow. Longer bake-out times up to two weeks are not uncommon.

- **Hydrogen Getter.** Using a hydrogen getter is the preferred tool for mitigation of H_2 poisoning. There are two basic types:

  - 1) metallized films that are welded to the lid
  - 2) molecular scavengers made with flexible polymer materials.

  Metallized films have the advantage of limited storage and handling concerns and no need for activation, but the molecular scavengers made with polymer materials have been proven to be more consistently effective. Polymer-based molecular scavengers can be easily sized and dimensioned for most any application, but there are critical requirements for their proper use. They convert the molecular hydrogen in the cavity to water and trap the water in a desiccant. Therefore, they require an "activation" at elevated temperature under vacuum to drive off adsorbed water. Once activated, they must not be exposed to ambient atmosphere because their effectiveness is diminished if internal moisture levels rise. However, the polymeric getters have high rates and high capacity for hydrogen adsorption and also act as moisture getters.

- **Vented Cavity.** In some cases, a completely nonhermetic cavity can provide a solution to hydrogen evolution from the cavity walls. Lack of hermeticity can lead to other issues, such as moisture or air sensitivity. A vented cavity may be susceptible to FOD (foreign object debris), sometimes of biological origin.

4.5 Operation in Vacuum

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
1 or as needed	1	once		✓		perform multipaction tests and/or analysis per TOR-2014-02198

If a nonhermetic device is operated in vacuum and the RF power level is substantial, then multipaction is of concern. Mulipaction is an effect that occurs in RF devices in vacuum or near-vacuum where free electrons are accelerated by an RF field toward metal electrodes. As the electrons collide with an electrode, secondary electrons are produced at each RF cycle in a resonant avalanche fashion that becomes destructive. Even in a hermetic package, with a typical leak rate, the multipaction effect can occur once sufficient time has elapsed for the internal sealing gas to have escaped. Depending upon the leak rates to which the packages have been qualified, there may be a near vacuum in a few months or a few years. Therefore, both hermetic and nonhermetic high RF power GaN applications must be addressed

for risk. A guideline for multipaction is TOR-2014-02198 (Graves, 2014), which provides specific details on whether testing or analysis is required. In general, a construction analysis on nonhermetic, vented, or PEM packages should be performed to check for the presence of voids, internal gaps, or other features subject to electron resonance. Multipaction testing may be required for space qualification in many cases. In other cases, qualification can be accomplished by analysis for Type 1 geometry (two surface metallic conductors) or Type 2 geometry (two surfaces with dielectric in line of sight). For Type 3 uncontrolled geometry or filled devices, testing will always be required.

5. Qualification for Extrinsic (Defect-Related) Failure Modes

Every fabrication process has a certain residual or unavoidable level of defects. The defects may be induced by airborne particles, contamination from various sources, or the vagaries of certain process steps such as metal liftoff or e-beam gate lithography. The objective of these tests is to ensure that the level of a fabrication process's extrinsic defects is understood and that their impact on the overall reliability is known.

Sometimes "intrinsic" defects—a bit of an oxymoronic term—are described. They are "built in" to the process and are captured in the tests of Section 3. Here the emphasis is on "extrinsic" defects that appear in a small fraction of devices causing "infant mortality."

Unlike wearout testing, which requires a relatively small number of samples stressed for long durations, testing for defects generally requires many devices stressed relatively quickly. Defect failure mechanisms tend to have decreasing failure rates as opposed to wearout mechanisms, which have increasing failure rates. The design or evaluation of screens requires that the defective population be established. The following tests are identified to target the typical defect mechanisms in GaN devices. The list may not be complete, and as more knowledge is gained, additional tests for specific types of defects might be necessary.

5.1 MIMCAP Qualification

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
500 min	all	continuously		✓	✓	• test structures recommended • tested area >1000× product area, divided into 500 MIMCAP test samples min. per Appendix F • all lots subject to continuous monitoring thereafter

MIMCAPs (metal insulator metal capacitor) are important components of MMICs and are used as DC blocks, bypass elements, filtering, etc. They often constitute a large fraction of the die area. In GaN devices, these capacitors are often exposed to fairly high voltages, unlike other MMIC technologies. Because of their large area and high voltage, they may actually dominate the reliability of a MMIC. MIMCAPs in a GaN process are typically fabricated with PECVD (plasma-enhanced chemical vapor deposition) silicon nitride as the insulating dielectric. A newer technique is ALD (atomic layer deposition), which uses gaseous precursors in a reactor and promises dielectric films with less defectivity. The thickness of this dielectric is a key to its reliability. The intrinsic reliability of typical MIMCAPs is usually far more than adequate for high-reliability missions. However, the presence of tiny defects in the dielectric film with much smaller "effective" thicknesses must be considered. It is this "extrinsic" reliability that dominates the overall MIMCAP reliability. It is recommended that ramped breakdown voltage tests on large numbers of large area samples be performed such that the total amount of MIMCAP area tested is at least 1,000× the area of MIMCAP in a product MMIC. The reliability of the MIMCAP may be determined from the ramp breakdown data. Because methods to convert this data into defect density—and thence into a reliability metric—have not yet been fully standardized, Appendix F is provided herein with an example reliability calculation for an example mission.

Appendix F shows one method to calculate the reliability using a TDDB (time-dependent dielectric breakdown) model based upon the Frenkel Poole current conduction model coupled with a charge-to-breakdown criterion (Scarpulla, 1999 & 2011). Another widely used model is the linear field bond-breaking model, also known as the "E-model," which has also been proposed (Yeats, 1998; Cramer, 2006). It, too, may be applicable although may not be as conservative.

To produce an accurate reliability assessment, a large amount of capacitor area must be devoted to destructive ramp breakdown testing. The tests are designed to determine the defect density of the MIMCAP process. The defects tend to dominate the reliability of MIMCAPs, not the bulk or intrinsic dielectric film. The desideratum, of course, is to have extremely low defect densities so that the MIMCAP failure rates in a typical space mission amount to just a few FITs. The measurements require large total areas of MIMCAPs to be devoted to testing. It is recommended that the total amount of capacitor area for ramp breakdown testing be at least 1000× the product MIMCAP area. In addition, it is recommended that this total amount of MIMCAP area be distributed amongst approximately 500 test capacitors at a minimum, each with an area 1/500 (maximum) of the total required. The test capacitors are each subjected to a destructive ramp voltage test. It is also recommended that the test capacitors be distributed across multiple wafer and lots, with at least three lots represented. All MMIC product should be analyzed for the sum of its MIMCAP areas and should be analyzed as necessary for different MIMCAP voltages.

Post-burn-in MIMCAP defect densities of less than about 50 defects/cm^2 are compatible with average failure rates of less than 20 FITs in typical missions of 15-year duration with typical MIMCAP areas. The failure distribution for MIMCAP defects decreases with time, unlike a wearout failure distribution. This means that given that a MIMCAP has survived for a certain length of time, its failure rate decreases with survival time. Therefore burn-in at elevated temperature and voltage is useful for MIMCAPs. It is recommended that as part of space qualification, the merits of the burn-in plan for the MIMCAP reliability be determined. The determination of the effectiveness of burn-in and pretesting to remove defects is shown in Appendix F.

In some GaN HEMTs, a field plate is added to reduce the electric field adjacent to the drain. This field plate is subjected to the highest voltages in the system, and the defects in this dielectric must be also qualified for long-term reliability. The dielectric in this field plate is also liable to have a certain defect density, characterized similarly to that in a planar MIMCAP. It is recommended that a similarly constructed MIMCAP be used to characterize the defect density in the insulator under the field plate. From there, the calculations are carried out exactly as in a conventional MIMCAP, as described in Appendix F.

5.2 Gate Defects

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
1000 equiv.	all	once, then ongoing		✓	✓	• test structures recommended • tested width equivalent to 1,000 DUTs • all lots subject to continuous monitoring thereafter

In GaN HEMT processes the formation of the gate electrode is critical. The gate is the finest lithographic feature of the entire HEMT device. It has a submicron gate length measured in tenths of a micron and a width of many millimeters. Power HEMTs have many gate fingers with a large total gate width.

Remarkably, the width-to-length aspect ratio is typically in the range of 10^3–10^5. The gate fingers are between the drain and the source. The high-voltage drain electrode is a few microns or less from the gate, and the source electrode is on the other side of the gate. Maintaining these small gaps, especially between the gate and drain electrodes, is important so that the device will have the desired high breakdown voltage and low leakage. Unfortunately, due to inevitable processing faults, defects of various types affect the gate electrode and the gate-drain or gate-source regions. The most serious defects are shorts between gate-drain or gate-source. Other types of defects are lifted gates, missing gate metal, or "bent gates," all of which prevent the device pinchoff in their vicinity, causing an increased subthreshold leakage. The purpose of the following test is to determine the preponderance or density of these defects.

It is recommended that two DC ramp voltages be successively applied to the gate-drain pair of electrodes (with source open) followed by the gate-source (with drain open). The ramps should be approximately 50 V/sec and be driven to the specified $V_{DSmax.safe}$ and $V_{GSmax.safe}$ voltages. The polarity should be such that the gate-channel is reverse biased in each case. Typically, the gate-source electrode pair has a lower reverse breakdown voltage than the gate-drain electrode pair. The voltage magnitude should be ramped or stepped and the current monitored, producing a ramped IV reverse diode characteristic for each electrode pair. The objective of this test is to observe the rare occurrences of shorts or high-leakage events. After many devices are tested, the density (per unit gate width) of these events is tallied up.

It is recommended that this test be performed on a total amount of gate width (the product of the number of HEMT gate fingers sample size and the gate width) no fewer than 1,000 times the typical product width. This testing may be performed at room temperature. Special wide gate or "fat fet" test structures are often used to reduce the number of actual samples and still meet this goal. The test structures may be on-wafer probed. For MMIC processes, the need for special test structures is evident. The defect density so characterized is a metric that will determine the likelihood of infant mortality HEMT failures and is useful in designing screens. It is important that this test be performed on unscreened devices for this reason. Once this initial qualification is performed, it is recommended that the tests be repeated in ongoing fashion with an appropriate frequency.

5.3 Airbridge Defects

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
12	3	ongoing		✓	✓	• open package or wafer • airbridge test structures recommended

Some GaN HEMT processes use Au electroplated air bridges as crossovers to feed the drain or gate electrodes in multifinger HEMTs. Airbridges are also used as crossovers for MIMCAPs and spiral inductors in MMIC layouts. The airbridge can have defects of various types, such as trapped contaminants beneath the airbridge, malformed or sagging airbridges, and broken airbridges. Some automated handling steps can be damaging to airbridges and should also be considered part of the entire fabrication process.

It is recommended that an airbridge bake test be performed for 1 hour at a temperature of 300 °C on a sample of 12 representative parts chosen from 3 lots. The test vehicle should be a product device or MMIC or an airbridge test structure expressly designed for this purpose. At a minimum, before and after the bake test, the airbridges should be inspected for problems or defects. There should be zero failures.

A more efficient approach would be to design an airbridge test structure consisting of a labyrinth of airbridges over metal conductors. A successful test is indicated by continuity through all the series-connected airbridges and no shorts to the underlying metal. The test structure can eliminate the need for optical or SEM inspections and allow monitoring of the process electrically. It is recommended that this test be performed on an ongoing basis with an appropriate frequency.

5.4 Via Defects

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
100× product via qty.	3	ongoing		✓		• open package • via test structure recommended

Vias (plated through or filled holes) are an advantage in microwave HEMTs and MMICs because they provide a low inductance path to ground for the active devices. This is important in achieving high-frequency performance. The backside via processing method and chemistry varies with the substrate type, typically SiC, Si, sapphire, etc. Dry etching of vias (Stieglauer, 2012) has been adopted at many GaN fabs. Via defects of various types can sometimes occur, for example, inadequately plated or improperly filled vias, cracked vias, or loss of continuity to the front or back metal. In some cases, inadequately cleared solvent or other chemical is present, causing corrosion or blowouts. The vias should be subjected to a temperature shock test followed by a bake to qualify them for high-reliability usage. The thermal shock simulates sudden changes in temperature that may occur during shipping of the system or the sudden temperature changes after launch. The bake test is then a stress to drive any defective vias toward failure.

It is recommended that a temperature shock test be followed by a bake test on vias. A representative product MMIC or HEMT can be used as a test vehicle. However, a dedicated test vehicle may be a more efficient way to access many vias. The test vehicle could consist of multiple vias or groups of vias that can be bonded or probed. It is recommended that a quantity of vias numbering approximately 100× the number found in a typical product MMIC or HEMT be used for qualification. For example, if a product die contains 30 vias, then the qualification should be performed on 3,000 vias. The test die should be drawn from at least three backside fabrication lots. With a dedicated test structure, the qualification process may be more convenient than using product die.

It is recommended that an air-to-air temperature shock test be performed with the temperature chambers set to –55 °C and +250 °C. This temperature range is wider than that usually specified for Si or GaAs tests because the anticipated maximum temperature of a GaN device is so much higher. The thermal mass of the test vehicle or chip mounting piece should be sufficiently small so as to allow the rate of change of temperature to be at least 50 °C per minute. There should be 50 thermal shock cycles. The dwell times at the hot and cold extremes should be 5 minutes. It is recommended that the thermal shock cycles be followed by a bake at 250 °C for 1 hour. The vias should be inspected optically at 30× magnification for cracks, delamination, bubbles, or other defects. If possible, the via electrical resistances should be measured before and after the thermal stresses. Any changes in resistance greater than 10% should be considered failures. No failures are acceptable. It is recommended that this test be performed in an ongoing fashion with a frequency appropriately chosen.

6. Qualification Tests for Mechanical Integrity and Packaging

Reliable packaging and the mechanical aspects of a high-power GaN HEMT or MMIC are important topics. For the die itself, the backside metal adhesion, frontside metal step coverage, die attach mechanical integrity, and wirebonding are all factors that can affect the long-term reliability. These items are covered here since they are directly associated with the wafer and die processing. Other issues having to do with the actual packaging method itself are equally important. Such issues are the die attach solder (or conductive epoxy) voiding fraction, the package hermeticity (or leak rate), surface mount package mechanics, micro-bump integrity, and many new issues associated with recent 3D or wafer-level packaging. Because these issues are related to the packaging technology and are somewhat independent of the GaN die or wafer process itself, they are out of scope in this guideline document. Figure 6-1 shows the die-related issues that are covered in this guideline. The tests referenced in the figure are for locations on, in, or directly adjacent to the die itself. If any failures occur, the root cause could possibly be traceable to the wafer fabrication rather than the packaging house.

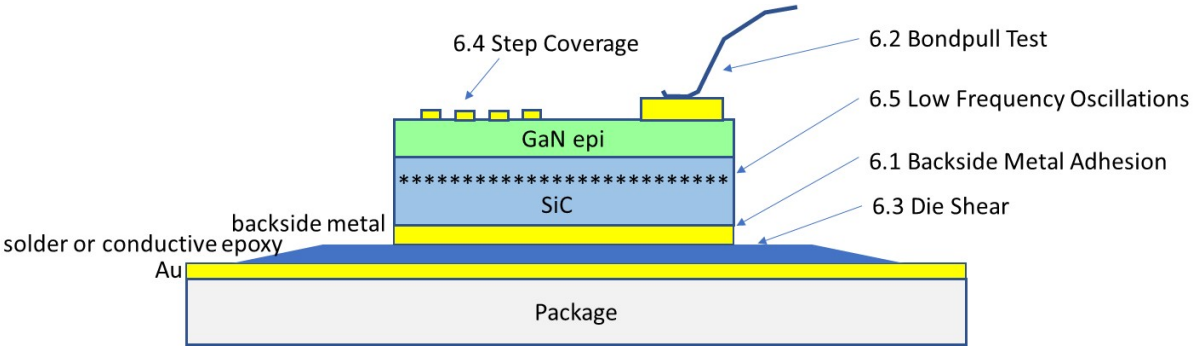


Figure 6-1. Illustrative GaN die mounted on a package base to illustrate the scope of mechanical and packaging issues covered in this section. All could be associated with the wafer fab rather than the packaging operation. (adapted from figure contributed by Cliff Burnett, Sumitomo Device Innovations, USA)

One potential problem area with certain semi-insulating substrates is the topic of low-frequency oscillations (LFOs). This issue is related to the starting material and substrate quality and is included in the final section here for completeness.

6.1 Backside Metal Adhesion

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
12	3	ongoing		✓	✓	mechanical fixture required

The substrates used in GaN HEMTs are usually SiC or (less commonly) sapphire or Si. The substrates are semi- or fully insulating. After wafer thinning, the backsides are sputter deposited with contact metallization, often multiple layers of material for adhesion. The back metal provides a ground plane and is part of the RF environment, being necessary to provide the counter-electrode for on-chip controlled impedance transmission lines, couplers, tuning stubs, etc. The adhesion of the back metal should be assured as part of qualification. Back metal adhesion testing is best performed using full or partial wafers or die with a relatively large area.

It is recommended that a simple tape pull test be implemented as a qualification check for the backside adhesion integrity. Although there is no test method or standard for a backside metal tape pull test, it is widely used, and it is quick and inexpensive. ASTM standard D3359-09 (2009) describes a pull test and may be used for guidance. This standard requires "cutting" of the film, either in an "X" pattern (method A) or a "crosshatch" pattern (method B), then affixing tape. For semiconductor wafers, it is recommended instead that the back surface metal be patterned in preparation for this test, either using a contact mask during back metal deposition or by patterning and etching the backside metal. It would also be acceptable to perform this test on unpatterned back metal. Adhesive tape (3M Inc. #600, ½ in. width Scotch Co., 2006) is affixed to the backside of the test piece. A mechanical fixture to hold the specimen is necessary. To pull the well-adhered tape off the specimen at a 180° angle requires approximately 44N/100mm (force per unit tape width). In this case with a ½ in.-(12 mm)-wide tape, the force required is 3.6 N. After the pull, the back of the specimen and the tape should be checked under a microscope at 15× magnification. There should be no removed metal on the specimen and no metal adhered to the sticky side of the tape. It is recommended that a total of 12 samples (4 samples from 3 lots) be tape-pulled. A passing qualification is that there is full adhesion of the metal film on the backside of the specimen. It is recommended that this test be performed in an ongoing fashion with an appropriately chosen frequency.

6.2 Bondpull Tests

These recommendations have been supplied by Robert D. Evans, Parts, Materials, and Processes Department, The Aerospace Corporation.

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
225 bonds	3	ongoing		✓		open package

The wire bonds in GaN technology usually consist of Au bonds to Au pads, a monometallic system. Wedge bonds or ball bonds are used to bond the device to the package or within the module. Gold wires bonded to a gold bond pad are extremely reliable because the bond is not subject to interface corrosion, intermetallic formation, or other bond-degrading conditions. The reliability issues tend to be related to contamination of the bond pads due to inadequate cleaning, leaving residue or films prior to bonding. Bondpull tests are the standard method used to evaluate bond integrity, and bondpull machines have been developed for the purpose. The problem with the standard methods is that they are adapted for a maximum ambient or die temperature of 125 °C or 150 °C. However, GaN parts will likely be operated to die temperatures of up to 200 °C or even 225 °C. Therefore, modifications to the standards are necessary.

It is recommended that the test standard "Bond strength (destructive bond pull test)," MIL-STD-883K change 3 Method 2011.10 (2018), be utilized with modifications. The modifications include multiple preconditioning bakes to accelerate any tendency for bond failure or weakening. It is assumed that early failure in the Au-Au system has an activation energy of 0.8 eV like the tacit assumptions found in military specification MIL-PRF-38534L (2019) Appendix C, para. C.6.3.2.4. This specification allows bondpull to be performed after a 1-hour 300 °C bake in air or in an inert atmosphere. Alternatively, this same military specification describes a QML qualification in Appendix C, para. C.7, which requires bondpull tests in para. C.7.5.4.11 after group C, steady-state life, which is 125 °C for 1,000 hours per Table C-Xc. From these two specific clauses, an activation energy of approximately 0.8 eV can be inferred, which is a typical value for wirebonding. The strategy for GaN wirebond qualification is to assume this same activation energy but tailor upward the temperatures and times.

The following procedure should be carried out in order to qualify a Au-Au wirebonding process for GaN die. Three groups of bondwires are to be tested. The BOL bond group simulates the beginning of life bonds, the EOL-1 group simulates a typical 15-year life, and the EOL-2 group simulates double this duration (i.e., 30 years).

1. For each of three different wafer lots, make 75 bondwires. This gives a total of 225 bondwires.

2. BOL bond group: Destructively pull 25 wires from each lot (75 wires total).

3. EOL-1 bond group: Precondition-bake 25 more wires from each lot (75 wires total) at 300 °C for 36 hours. Destructively pull the 25 wires.

4. EOL-2 group: Precondition-bake the final 25 wires from each lot (75 wires total) at 300 °C for 72 hours. Destructively pull the 25 wires.

The data is in units of grams force. Compute the mean and standard deviation of the BOL, EOL-1, and EOL-2 groups. For the three sets of data, compute the one-tail 99% confidence level (mean minus 3.1 standard deviations). The qualification of the bondwires passes if the result exceeds the values in the graph of Fig. 2011-2 of MIL-STD-883K (2018) Method 2011.10 "Minimum bondpull limits." For the BOL-1 group, the "Au preseal" values should be used. For the EOL-1 and EOL-2 groups, the "Au post-seal" values should be used.

Representative die should be etched to assure that the wirebonding process has not damaged the bulk die material under the wirebonding pads. Optical inspection of approximately 3 bondpads from any of the above samples at 15× should be performed. There should be no evidence of cracking or damage to the underlying material.

It is recommended that bondpull tests be performed on product devices as dictated by the reliability needs of the mission. Also, a program of monitoring the bonding equipment is recommended by performing this test on an ongoing basis with a frequency appropriate to the process.

6.3 Die Shear Tests

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
6 die	3	ongoing		✓		mounted die

The procedures called out MIL-STD-883K Method 2019.10 (2018) should be followed to the letter. The failure criteria given therein should be followed. The sample size should be 2 die from each of 3 bonding lots, for a total of 6 die shear tests. There should be no failures. It is recommended that this test be performed in an ongoing fashion with an appropriately chosen frequency.

6.4 Step Coverage

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
6-12	3	ongoing		✓	✓	open package

The provisions of MIL-STD-883K (change 3), Method 2018.6 (2018) with regard to SEM inspection of Class S devices should be followed for metal step coverage. Depending upon the type of metal deposition, Method 2018, Table I shows the number of sample wafers required to be inspected. The samples may be full wafers or die with the necessary features. For example, the table specifies that for a planetary wafer holder system, two wafers are required to inspect metal steps whether from a sputter deposition system or an evaporator. For other types of wafer holders, the sampling is more complex. Typical sampling is 2–5 DUTs or wafers from each of 3 lots for a total of between 6 and 16 DUTs. Electroplated metals, often found in GaN processes, are not included in Method 2018.6. It is recommended that 3 samples per lot (9 DUTs total) be inspected for electroplated metals. It is recommended that this test be performed in an ongoing fashion with an appropriately chosen frequency. It is also recommended that the many SEM images be scrutinized, showing accept and reject examples, as many are quite applicable to GaN MMICs and transistors. These SEM images have recently been added to MIL-STD-883K (change 3).

6.5 Low-Frequency Oscillations (LFOs)

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
3	3	once, or upon changes in substrate(s)	✓	✓		product die

In the past, the semi-insulating substrates used in GaAs technologies have suffered from the problem of low-frequency oscillations. The mechanism is not fully understood but believed to be related to the time constants for traps in the substrate under space charge limited current flow (Makram-Ebeid, 1985; Miller, 1987). For GaN transistors (usually with SiC semi-insulating substrates), low-frequency oscillations have not been reported. The purpose of this test is to eliminate this concern.

It is recommended that representative GaN HEMTs or MMICs be used as a test article, with the full backside process in place. The device should be biased off with gate voltage V_{GS} more negative than the pinchoff voltage. The drain voltage V_{DS} should be set to the maximum off state safe or derated value and be connected to the drain terminal through a high-value ballast resistor. The value of the resistor is determined by the leakage current at the specified voltage. The voltage drop across the ballast should be no more than 1% of the applied voltage. A dynamic signal analyzer or noise analyzer is used to measure the low-frequency noise spectrum in the range of 0.01 Hz to 1 kHz. There should be no peaks or spurious low-frequency oscillations in the noise spectrum. The noise spectrum should otherwise have a typical smooth, decreasing noise density as a function of frequency. It is recommended that three representative devices be tested, each from a different substrate lot or production lot.

This test should be conducted once for a given substrate type and vendor. If substrates are sourced from a different supplier, or if substrate specifications are changed, it is recommended thatt this test be repeated.

7. Radiation Tests

This section contains contributions from Joseph R. Srour, Electrical Systems Assurance Department, The Aerospace Corporation.

Like many III-V electronics, GaN has proven to be remarkably radiation hard to most types of radiation. In many space missions, such as in LEO (low Earth orbit), or for short durations, space radiation environments may be modest. In these environments the effects on GaN HEMTs and MMICs tend to be relatively small. In other situations, this may not always be true. The tests described in this section are recommended to qualify the design of the GaN device or technology for the intended radiation environment.

The following topics are discussed next. In Section 7.1 is a discussion on radiation sensitivity and in Section 7.2 the need for RLAT (radiation lot acceptance testing) of GaN HEMTs and MMICs. In Sections 7.3 to 7.6, the various radiation environments are discussed. In Section 7.7, for the various radiation environments, specific example test plan outlines are provided with testing recommendations, DUT quantities, procedures, and caveats summarized. These test plans may be tailored to the specific space application and environment of interest. The topics are:

- Radiation Sensitivity of GaN HEMTs and MMICs
- GaN Radiation Lot Acceptance Testing (RLAT)
- Total Ionizing Dose (TID)
- Ionizing Dose Rate
- Single-Event Effects (SEE)
- Displacement Damage (DD)
- Example test plans

In Appendix G the following topics are provided for additional information:

- Supplemental Information
  - TID testing considerations for GaN in space applications
  - Ionizing dose-depth comparisons of GaN to other technologies
  - Dose enhancement considerations for GaN
  - Relative GaN displacement damage sensitivity
  - Heavy ion interactions with GaN HEMT devices

7.1 Radiation Sensitivity of GaN HEMTs and MMICs

GaN devices have proven to be quite radiation hard to most types of radiation, which is the case for many III-V-based electronic devices. For moderately short satellite missions in LEO, for example, natural radiation effects are minimal. For longer GEO missions or those with manmade radiation, there are some observed effects that can be attributed to the HEMT or MMIC design. Consequently, several types of radiation testing should be conducted to qualify the design of GaN transistors for space use. The interim tests and failure criteria of Sections 3.5 to 3.7 should be applied to pre- and post-irradiation measurements. Trap characterization measurements such as those described in Section 3.6 are especially recommended. Additionally, recommendations for radiation effects mitigation techniques (shielding, redundancy, GaN process changes, etc.) should be made, and an end-of-life (EOL) performance estimation should be provided for the intended mission lifetime.

Various radiation testing procedures and related guidelines have been developed by the DOD, NASA, JEDEC, ASTM, ESA, The Aerospace Corporation, and Sandia National Laboratories for evaluating electronic parts intended for use in radiation environments. These guidelines are listed here (see References for citation details):

- DOD
  - MIL-PRF-19500P, w/ Amendment 4, *Performance Specification: General Specification for Semiconductor Devices* (2018).
  - MIL-PRF-38535L, *Performance Specification: Integrated Circuits (Microcircuits) Manufacturing* (2013).
  - MIL-STD-883K, Method 1017.3, *Neutron Irradiation* (2015).
  - MIL-STD-883K, Method 1019.9, *Ionizing Radiation (Total Dose) Test Procedure* (2015).
  - MIL-STD-883K, Method 1020.1, *Dose Rate Induced Latchup Test Procedure* (2015).
  - MIL-STD-883K, Method 1021.3, *Dose Rate Upset Testing of Digital Microcircuits* (2015).
  - MIL-STD-883K, Method 1023.3, *Dose Rate Response and Threshold for Upset of Linear Microcircuits* (2015).
  - MIL-STD-750-1A, Method 1017.1, *Neutron Irradiation* (2016).
  - MIL-STD-750-1A, Method 1019.5, *Steady-State Total Dose Irradiation Procedure* (2016).
  - MIL-STD-750-1A, Method 1080.1, *Single-Event Burnout and Single-Event Gate Rupture* (2016).
  - MIL-HDBK-814, *Ionizing Radiation and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices* (1994).
- NASA
  - NASA Technical Memorandum 4527, *Natural Orbital Environment Guidelines for Use in Aerospace Vehicle Development* (Anderson, 1994).
  - NASA/Goddard Space Flight Center, *Proton Test Guideline Development—Lessons Learned* (Buchner, 2002).
- JEDEC
  - JEDEC Standard JESD57A, *Test Procedure for the Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation* (2017).
  - JEDEC Standard JESD234, *Test Standard for the Measurement of Proton Radiation Single Event Effects in Electronic Devices* (2013).
- ASTM
  - ASTM E1249-15, *Standard Practice for Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co-60 Sources* (2015).
  - ASTM F1892-12, *Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices* (2012).
  - ASTM F1893-11, *Guide for Measurement of Ionizing Dose-Rate Survivability and Burnout of Semiconductor Devices* (2011).
  - ASTM F1262M-14, *Standard Guide for Transient Radiation Upset Threshold Testing of Digital Integrated Circuits*, July (2014).
  - ASTM F1263-11, *Standard Guide for Analysis of Overtest Data in Radiation Testing of Electronic Parts* (2011).
  - ASTM E1854-13, *Standard Practice for Ensuring Test Consistency in Neutron-Induced Displacement Damage of Electronic Parts* (2013).
  - ASTM F980-16, *Standard Guide for Measurement of Rapid Annealing of Neutron-Induced Displacement Damage in Silicon Semiconductor Devices* (2017).
  - ASTM E722-14, *Standard Practice for Characterizing Neutron Fluence Spectra in Terms of an Equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics* (2014).

  - ASTM F1192-11, *Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices* (2011).
- ESA
  - ESA-ESCC-22900, *Total Dose Steady-state Irradiation Test Method*, October 2010.
  - ESA-ESCC-25100, *Single Event Effects Test Method and Guidelines*, October 2014.
- The Aerospace Corporation
  - TOR-2006(8583)-5236, Revision B, *Technical Requirements for Electronic Parts, Materials, and Processes Used in Space and Launch Vehicles* (Robertson, 2013).
- Sandia National Laboratories
  - *Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Test Guideline for Proton and Heavy Ion Single-Event Effects* (Schwank, 2013a).
  - *Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance* (Schwank, 2013b).

The primary emphasis in this documentation is on methods for performing radiation testing of Si devices and circuits because of their predominance in space and military systems. Note that MIL-STD-750 is intended specifically for discrete semiconductor devices, while MIL-STD-883 covers a more general spectrum of microelectronic devices, including monolithic, multichip, film and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. Where similarly designated test methods (e.g., test method 1017 for neutrons) appear in both standards, care should be taken to properly apply them to the devices of interest. Some of the radiation test procedures called out in these many standards also explicitly apply to testing of GaAs devices.

The general question arises regarding GaN devices (rather than Si or GaAs): What procedures should be implemented when performing radiation evaluation and qualification of GaN devices for use in military and space applications? It is likely that most of the presently employed test procedures can be tailored to be applicable to GaN devices. In some cases, very little tailoring may be needed. Initial recommendations are given here regarding the tailoring that is likely to be appropriate for radiation testing and qualification of GaN devices for use in the following natural and manmade radiation environments: total ionizing dose; ionizing dose rate; single-event effects; displacement damage. In the following sections, some example qualification strategies for various radiation environments are also provided. These may be used directly or tailored appropriately for the specific application under consideration.

7.2 RLAT for GaN Devices

Radiation effects evaluation of electronic parts typically includes two stages. The first is often referred to as characterization (or engineering) testing, and the second is radiation lot acceptance testing (RLAT). For a specific part type, such as a GaN HEMT, key examples of characterization testing involve screening that part to examine degradation in environments that deposit total ionizing dose (TID) and produce displacement damage. One outcome of characterization testing may be revealing, for example, that a given part type is relatively insensitive to degradation in a TID environment. Depending on the dose levels involved, that insensitivity might provide the basis for exempting a specific part from TID RLAT for some programs. RLAT evaluation involves testing flight-lot parts in a specific radiation environment to program-required levels. For example, a program might specify that parts must meet performance requirements after receiving a TID of at least twice the expected dose to be received by a shielded part in space applications. Guidelines on the need for RLAT and the criticality ratings of devices are found in MIL-HDBK-814 (1994). If RLAT is needed, it may not be necessary to include all the types of radiation testing, depending upon the mission requirements. Only single-event tests, for example, may be needed but not TID or DD tests.

At the time of this writing, there are no RF GaN transistor or MMIC RLAT programs contemplated or underway for Class A or B satellite missions. This state of affairs exists because GaN HEMTs are relatively radiation hard as compared to the radiation requirements of many space missions for which they are presently being considered. At this time, very few (if any) GaN devices have been qualified for space in the first place. The avowed purpose of this document is in fact to provide some guidelines toward that end. In order to qualify a device for a mission that has a radiation environment, it must be fully characterized. Detailed suggestions for such characterizations are provided below for the various radiation environments. A determination must then be made as to the sensitivity of the device to these radiation environments. At this point, the understanding is that the devices generally are sufficiently rad hard to all the typical relevant environments so as to obviate the need for RLAT. Therefore, the emphasis in the paragraphs below is toward characterization rather than the establishment of an RLAT plan.

This situation is not unlike the case for GaAs HEMT devices that are considered to be "intrinsically" radiation hard. (This is a familiar and operative misnomer—with sufficiently high radiation dose or fluence, any device can fail.) The failure levels for GaAs devices is understood to be very high as compared to many mission needs. This also may well be true for GaN HEMTs and MMICs. Therefore, in the paragraphs to follow, emphasis is on the characterization phase of qualification rather than RLAT. In those cases where radiation levels are very high, or if a GaN device appears to be very radiation soft, the RLAT guidelines of MIL-HDBK-814 (1994) should be followed.

7.3 Total Ionizing Dose

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
40	3	per MIL-HDBK-814	✓	✓		performed only once if RDM is sufficient for mission

In general, the effects of ionizing radiation on electronic devices are important in the natural space environment and in manmade environments. Guidelines for qualification testing of GaN devices for total ionizing dose (TID) effects are considered here. General comments applicable to the TID testing of parts for space use are provided in Appendix G, including ionizing dose deposition and dose enhancement considerations.

The GaN HEMTs under consideration do not contain gate-insulating layers as a key constituent of their device functionality (e.g., MIS-HEMTs are not considered). Early work indicated GaN devices to be relatively radiation tolerant in terms of their TID response. However, recent work shows some non-MIS GaN HEMT devices to be moderately sensitive not only to TID but also to displacement damage effects (Jiang, 2017). That work highlights the need to test GaN devices under various operating conditions during radiation qualification testing.

Existing standards and guidelines for performing TID testing are primarily designed for Si devices. The *general* aspects of total dose testing given in those documents are applicable to GaN devices, but the *specific* testing conditions will need tailoring and will depend on the type of GaN device being examined. The standard approach to TID RLAT is to perform irradiations using a Co-60 gamma-ray source.

GaN device-specific electrical measurements must be made before and after each TID irradiation. Measurements and failure criteria should include those of Sections 3.5 to 3.7 for transistors, including power, RF gain, and PAE for MMIC amplifiers. Trap characterization measurements of Section 3.6 are especially recommended. Pre- and post-irradiation measurements need to be taken while operating at the

intended operational frequency. During TID exposure, operating conditions should be typical of those for the intended space application. Also, consideration should be given to examining worst-case operating conditions, such as DC bias effects during irradiation. Degradation of Si_3N_4 layers due to TID irradiation also needs to be accounted for. In general, for space missions, a goal is to observe no GaN device failures up to an ionizing dose of 1×10^6 rad (GaN).

The minimum number of DUTs to irradiate in a specific operational state is five plus one unirradiated control device. As discussed in Section 7.2, RLAT testing for Si devices involves first performing neutron irradiation to a fluence level of programmatic interest, which is generally followed by TID testing on that same set of samples. After this irradiation sequence is completed, the combined results of displacement damage and ionization-induced damage are obtained. In this conventional RLAT approach, it is important that all devices receiving TID irradiation have previously been irradiated with neutrons. If it becomes clear through characterization testing for a specific type of GaN device that TID irradiations are needed for more than one operating condition, then the number of samples needed for neutron RLAT should increase. For example, it might be necessary to perform unbiased and biased TID irradiations if such devices are known to exhibit bias dependences. The main point for RLAT is that the number of samples to be neutron irradiated must be the same as that for subsequent TID irradiations of the same samples.

The following test conditions are recommended for TID qualification: five DC biasing conditions (the Q-points Q1–Q4 of Figure 3-1 plus one unbiased case) and two operational conditions typical of an intended space application, for example, two frequencies or two different power levels. A minimum of five devices is also recommended for each of those seven cases. Therefore, a total DUT count of 40 devices is needed (5 devices × 7 cases plus 5 controls).

If it is found that the devices have an additional sensitivity to displacement damage at proton or neutron fluences of programmatic interest, then the TID DUT quantity of 40 may be inadequate. The worst-case scenario would be that all the TID testing noted above would need to be performed a second (or even a third) time. A repeat would be needed with a set of DUTs that had previously been exposed to at least 1× mission fluence (or perhaps a second repeat at 2× or higher). Therefore, the maximum number of DUTs needed could be as high as 80, or even 120. (Based upon recent results (Harris, 2011; Ives, 2013; Weaver, 2012 & 2016) the fluences needed to cause significant displacement damage effects are relatively high, typically beginning at about 10^{12}–10^{13} n/cm^2, and these precautions may well be unnecessary in many cases.) It is likely that by the time the information about displacement damage effects are discovered, it will be accompanied with the knowledge of the most sensitive bias condition. Therefore, it may not be necessary to repeat all the test cases.

7.4 Ionizing Dose Rate

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
14	3	per MIL-HDBK-814	✓	✓		• Operate-through test • performed only once if RDM is sufficient for mission
14	3	per MIL-HDBK-814	✓	✓		• Survival test • performed only once if RDM is sufficient for mission

One effect of a manmade radiation event is the production of a short burst of ionizing radiation, resulting in a high dose–rate environment. In general, that environment can cause three effects in electronic

devices: transient upset, latchup, and burnout. Latchup is not expected to occur in GaN HEMTs due to the lack of a pnpn path with associated parasitic bipolar transistors having sufficient current gain to sustain that process. Transient upset refers to any temporary increase in current or voltage that occurs due to the incident-ionizing burst. Whether such transients are an issue for a given GaN device depends on the duration and magnitude of the transient, the specific application for that device in a space mission, and the program operational requirements. Burnout can occur at high dose rates due to local thermal effects induced by the accompanying high currents. GaN devices should be examined for such an effect. GaN devices fabricated on a Si substrate may have more dose-rate response than with GaN on semi-insulating (native GaN, SiC, etc.) substrates.

Existing standards and guidelines for performing ionizing dose–rate testing are primarily designed for Si devices. The *general* aspects of dose-rate testing given in those documents are applicable to GaN devices, but the *specific* testing conditions will need tailoring and will depend on the type of GaN device being examined.

It is recommended that GaN device-specific electrical measurements be made before and after ionizing dose–rate testing. Measurements and failure criteria should include those in Sections 3.5 to 3.7 for transistors, power, RF gain, and PAE for MMIC amplifiers. Trap characterization measurements such as described in Section 3.6 are especially recommended. During dose-rate testing, operating conditions should be typical of those for the intended space application of a given device. Also, consideration should be given to examining worst-case operating conditions.

For missions with an *operate through* requirement, it is necessary to demonstrate under increasing dose rates that the DC and RF performance of the GaN device does not permanently degrade beyond failure criteria up to an example rate of 1×10^{10} rad/sec and that the power output recovers in < 1 μsec. For missions with a *survive and recover* requirement, it is necessary to demonstrate that the GaN device DC and RF performance does not permanently degrade beyond failure criteria and experiences no catastrophic failures or burnout under operational conditions (i.e., amplifying power or RF) up to an example dose rate of 1×10^{12} rad/sec. Power output recovery in < 1 sec again is an example goal. In general, most GaN power HEMT devices generate much less dose rate–induced current than Si devices do, such as MOSFETs of similar voltage and current rating. See Appendix G, Section G.2 for more details.

Dose-rate evaluation typically involves using flash xray or electron LINAC (linear accelerator) facilities. The number of devices needed for such testing depends primarily on the number of dose rates to be examined and the operational conditions appropriate for a given device. The preliminary estimate given here assumes that transient upset and burnout measurements will be performed at six dose rates. It is also assumed that two operational conditions are explored at those dose rates. For dose rate tests, it is recommended that two Q-points of Figure 3-1 be selected: Q1 (central in the IV plane) and Q4 (maximum voltage). The DUTs may be exposed to the six dose rates successively, as long as the total dose per exposure is not excessive compared to their TID sensitivity. Generally single-shot exposures should be performed at flash xray and LINAC facilities so as to control the accumulated doses. It is recommended that at least 5 DUTs be devoted to each of the two Q-points, along with 4 controls. A recommended minimum of 14 DUTs are for ionizing dose rate tests.

7.5 Single-Event Effects (Protons and Heavy Ions)

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
up to 66	3	once	✓	✓		delidded or open package required for heavy ions

In general, single-event effects (SEE) on electronic devices and circuits include several effects: single-event upset (SEU), single-event transients (SETs), single-event functional interrupt (SEFI), single-event latchup (SEL), single-event burnout (SEB), single-event gate rupture (SEGR), and single-event dielectric rupture (SEDR). Three of these effects are nondamaging (SEU, SET, and SEFI), and the remaining four can be destructive (SEL, SEB, SEGR, and SEDR).

Experimental and analytical studies of single-event effects (SEE) in GaN devices have been conducted for several years, but the breadth and depth of such efforts are quite low compared to Si devices. For examples of recent SEE studies on GaN devices, see Kuboyama (2011), Rostewitz (2013), and Armstrong (2015) and citations therein. Existing standards and guidelines for performing SEE testing are primarily designed for Si devices. The *general* aspects of SEE testing given in those documents are applicable to GaN devices, but the *specific* testing conditions will need tailoring and will depend on the type of GaN device being examined.

In Si devices, the relatively high proton fluences that occur in certain LEO or MEO (low or medium Earth orbit) satellite orbits are capable of creating both direct ionization and secondary ionization. Direct ionization does not pose much of a risk in typical devices because the proton LET is relatively low. However, approximately 1 proton in 10^5 will undergo a nuclear reaction with the silicon composing the bulk of the device. These nuclear reactions can produce heavy ions of various atomic numbers up to that of Si ($Z = 14$) that in turn can deposit enough energy to cause upset in a Si-based memory cell, for example. In GaN devices it is believed that similar behavior may occur (Khanna, 2004; Pearton, 2016); however, the details of the secondary heavy ions, their atomic numbers, and LETs have not yet been worked out. However, it may be true that the same logic holds for GaN as for Si as follows: If a proton undergoes a nuclear reaction with a Ga atom in the lattice, it can produce a Ge ion (Ga + proton = Ge). This is the most unfavorable result. (The proton can also generate spallation products of lower atomic numbers that are fragments of the original Ga atom. Since these are lighter, the LET will be smaller. Therefore, Ge is worst-case). If heavy ion tests show that Ge ions of various energies produce no SEE or SEB, then proton testing would have no effect. In other words, if the threshold LET is higher than can be achieved with Ge at energies available at cyclotron facilities, then proton testing would not be expected to be useful. It remains to be seen if this logic holds up.

See Appendix G for further considerations regarding differences in LET depending upon the target GaN, AlGaN, SiC, etc., as compared with Si. These differences now necessitate keeping track of and acknowledging the target material. It cannot be assumed that the LET for a Si device is identical to that in an AlGaN/GaN HEMT device. For this reason, in this document, LET is expressed in units of MeV-cm^2/mg (GaN) to explicitly indicate this material dependency. It is recommended that the LET for the material stackup(s) of the particular device along with overlayers be analyzed with an ion transport program such as SRIM™ (Ziegler, 2008).

Luckily most GaN HEMTs and MMICs of interest are RF power devices with relatively large physical active areas, consisting of wide gate, drain, and source fingers. The total effective device width can be 10 mm or more in a power HEMT or MMIC. When an ion strike occurs, the area affected is far less than 1 μm^2 and is small compared to the area of a full device. Charge collection experiments using single photon

absorption (SPA) employing a UV laser, two-photon absorption (TPA), ion microbeams, and xrays (Onoda, 2013; Koehler, 2017; Katchatrian, 2017 & 2019) have been performed. The charge collected is relatively small compared to the charge that moves by normal conduction between drain and source in a device having a useful width. The SEU event therefore consists of a relatively small current transient. The transient varies from less than 1 mA to about 20 mA, depending upon device construction and the radiation beam deposition characteristics. The duration of the transients is about 100–200 psec, with long tails up to 1 msec observed under certain bias conditions. The long tails are believed to be due to traps that collect the liberated charge from the ion track and release it slowly. These are likely the same traps causing current collapse and phase noise. In addition to the small transients, damage is observed indicated by increases in leakage current and degradations in output power and gain (Kuboyama, 2011; Armstrong 2015; Olson 2015). The saturated cross sections for these transients have also been found to be slightly larger than the geometrical cross sections of the space between the drain and source (Rostewitz, 2013). No latchup has been observed in GaN HEMTs with Schottky gates, even those fabricated on Si substrates.

On the other hand, it has been shown that SEB (single-event burnout) can occur in power GaN devices (Martinez, 2019). Little open literature exists on SEB for GaN RF/microwave HEMTs and virtually none on GaN MMICs. This is because power-switching devices have garnered more attention, especially since many have much higher working voltages. High voltages always cause misgivings in a system exposed to cosmic rays. In both power GaN devices (with Schottky gates) and GaN RF/microwave devices, the burnout is not a latchup but rather is like the usual off-state catastrophic breakdown. The breakdown appears to be initiated by the charges introduced by the strike while the high voltage is applied to the drain (Bazzoli, 2007; Scheick, 2017; Martinez, 2019). Burnout tests have revealed the following general trends:

- For a given HEMT process, a larger device is more prone to SEB than a smaller one operated at the same current and power density. Its SEB cross section is higher and presents a higher Poisson probability of failure.

- A higher-voltage and lower-current HEMT will tend to burn out more readily than a lower-voltage and higher-current one rated for equal RF output power. It seems that a higher voltage is the key factor.

- It is believed that a HEMT operated under large signal RF conditions is more prone to SEB than the same HEMT subjected to DC voltage only. There is uncertainty in this belief since the RF peak voltages may not always be as well understood as an applied DC voltage. It is unknown if the presence of the RF signal itself enhances SEB or if it is merely that an RF voltage (or electric field) peak exists at the instant of the ion strike.

- SEB has been observed in the active region of the HEMT near the 2DEG and in the substrate near the drain. There may well be multiple sensitive regions, each with a different SEB cross section. It is believed that with sufficient derating of the peak voltage, SEB may be eliminated. This may necessitate derating the drain voltage to values lower than the $V_{DSmax.safe}$, otherwise deemed acceptable by electrical considerations alone (see definitions in Section 2).

- Unexpected burnout from SEDR in proton testing has been found recently in MIMCAPs having a dielectric thickness of 100 nm fabricated in a Si process. The MIMCAPs were destroyed only when DUTs were housed in packages containing Au plating typical of microwave housings (Turflinger 2015 & 2017). The protons cause a fission reaction in the Au atoms, and some fragments knocked off may have sufficient LET to cause SEDR. This effect may have serious implications in a GaN device where Au is used not only in the packaging but also for the

metallization used on the die itself. In a proton-rich radiation environment, the presence of the Au packaging and metallization may be a very important factor for MIMCAPs used in GaN MMICs.

It is recommended that GaN device-specific electrical measurements be made before and after SEE testing. Measurements and failure criteria should include those of Sections 3.5 to 3.7, especially including power, RF gain, and PAE for MMIC amplifiers. Trap characterization measurements such as described in Section 3.6 are especially recommended. During SEE testing, operating conditions should be typical of those for the intended space application of a given device. Also, consideration should be given to examining worst-case operating conditions. For example, measurements should be obtained while amplifying at the intended operational frequency. In addition, examining the impact of relevant or slightly elevated DC biasing conditions on SEE behavior should be considered. For operational space missions, an example goal is that there should be no SEE-induced failures up to a linear energy transfer (LET) of 75 MeV-cm^2/mg (GaN). Finally, some attention should be given when field plates are employed in the HEMTs. Field plates connected to the source (usually ground) electrode shield the gate from the higher voltage drain electrode. The field plate is separated from the gate metal by an insulator, typically Si_3N_4, which is exposed to a high electric field. When subjected to heavy ions, this insulator can break down, creating a SEDR (single-event dielectric rupture) effect somewhat similar to single-event gate rupture in Si power MOSFETs. It has also been observed that the gate leakage current I_{gLeak} gradually increases with exposure to heavy ion fluence (Armstrong, 2015). This leakage may be a result of damage in the field plate insulator or in the intrinsic HEMT itself.

SEE evaluation includes testing with heavy ions and protons. Heavy-ion testing involves bombarding parts with various ions having a range of LETs, and proton testing is performed at several proton energies. Recommending the number of devices needed for SEE testing depends on three variables:

1. the number of irradiation conditions (ion LET, proton energy) that need to be examined at heavy-ion and proton test facilities

2. the specific phenomena anticipated to be observed for a given device (i.e., SEU, SET, SEFI, SEL, SEB, SEGR, and SEDR)

3. the operational conditions of interest for a given device

The preliminary estimate given here assumes that several of the general types of single-event effects (e.g., SEU, SEL, and SEGR) are not an issue for conventional GaN HEMTs. It is also assumed that heavy-ion testing is conducted at six LETs and proton testing includes four proton energies. Further, it is assumed that two operational conditions are explored. If a minimum of three devices are tested at each ion LET and at each proton energy, for two operational conditions, then a minimum of 60 DUTs would be needed. It is also recommended that approximately 6 controls be included, bringing this quantity to 66 DUTs.

7.6 Displacement Damage

# DUTs	# Lots	Frequency	Configuration			Notes
			Hermetic	Nonhermetic	Wafer	
8	3	once	✓	✓		passively irradiated

Displacement damage effects on GaN devices have been examined by various workers. In one study of fission neutron effects on LEDs (Li, 2003), significant changes in device properties did not occur until

after a relatively high fluence (1×10^{14} n/cm^2). Observed effects were attributed to carrier removal. Four example studies of displacement damage effects in GaN HEMTs found very good radiation tolerance (Roy, 2010; Weaver, 2012 & 2016; McCurdy, 2017). However, recent work indicates some susceptibility to displacement damage in GaN HEMT devices (Jiang, 2017) from protons under semi-on and on-state bias conditions. In terms of displacement damage effects, the indication is that GaN devices may be good candidates for use in applications with significant radiation environments. For example, GaN is a direct bandgap semiconductor material, so it is relatively insensitive to minority-carrier lifetime reduction via displacement damage as is the case for GaAs (discussed in Appendix G). Studies have been made to determine the mechanisms responsible for the tolerance of GaN devices to displacement damage effects (Roy, 2010; Weaver, 2012 & 2016; Pearton, 2016). At high fluences, traps (donors or acceptors, depending upon the fluence) are generated in the AlGaN and GaN layers at the heterojunction, and the threshold voltage and transconductance are affected (Ives, 2015).

Displacement damage effects in Si and GaAs devices are independent of applied bias during irradiation. For GaN HEMTs, it is assumed that neutron irradiations should be performed with all devices unbiased. Providing biasing and other operational modes during neutron bombardment is far more complicated than for TID irradiations. Displacement damage irradiation involves using either a fission nuclear reactor or a monoenergetic source of 14-MeV neutrons. This standard approach allows the separate effects of ionizing and nonionizing radiation to be determined since neutrons deposit negligible ionizing dose. It is recommended to accrue the fluence in a stepwise fashion using a set of six DUTs (plus two controls) from three lots dedicated to the purpose, performing interim measurements and using failure criteria as described in Sections 3.5 to 3.7 up to at least 2× the fluence of program interest. Trap characterization measurements such as described in Section 3.6 are especially recommended. It is recommended that at least 4 fluence steps be taken. All measurements should be taken while amplifying at the intended operational frequency. For space missions, a typical goal is to observe no device failures up to fluence of 1×10^{12} n/cm^2 (1-MeV-equivalent Si).

Space programs generally include radiation requirements for displacement damage expressed in terms of a 1-MeV-equivalent neutron fluence versus Al shielding thickness. The damage produced in Si by energetic electrons and protons in an orbit of interest is determined first. Then the fluence of 1 MeV neutrons that would produce the same amount of damage in Si is determined, using the standard ASTM method F980-16 (2017) in conjunction with NIEL scaling (e.g., Srour, 2013 and citations therein). NIEL for GaN is discussed in Appendix G of this document. The ASTM standard E722-14 (2014) also includes information on expressing an equivalent amount of damage in GaAs and Si. The present view is that since space programs generally express their displacement damage requirements in terms of a 1-MeV-equivalent-Si neutron fluence, for displacement damage testing of GaN devices it is sufficient to expose them to a Si-determined equivalent fluence. There does not appear to be a need to express that fluence in terms of the equivalent damage produced by 1-MeV neutrons in GaN.

In summary, testing of GaN devices for radiation-induced displacement damage effects generally can follow existing standards for Si devices since such effects are assumed to be independent of operating conditions during bombardment (i.e., irradiate all samples unbiased). The pre- and post-irradiation measurements noted above to be performed on GaN devices are tailored to the specific type of device being evaluated.

7.7 Example Radiation Qualification Test Plans

The following paragraphs provide some basic radiation effects test strategies for GaN HEMTs and MMICs in the various radiation environments. These plans are shown here as a starting point for tailoring by space programs. It is highly recommended that tailoring of these basic plans be performed based upon the actual mission radiation environments, the mission reliability goals, and performance requirements.

Sufficient variability exists in radiation environments, device packaging, overlayers, amount of spacecraft shielding, etc., to make it impossible to provide a rigid guideline or test specification here. It is the aim of this section to provide users with an awareness of the test methods and their implications.

7.7.1 Radiation DUT Sample Size

Based upon the discussions provided in the above sections, recommended DUT sample sizes for each type of GaN radiation qualification test are shown in Table 7-1. These sample sizes are based upon a quantity of 5 DUTs for each experimental test condition (with the exception of SEE tests, requiring numerous test conditions, where only 3 DUTs per condition are recommended in the interests of practicality).

Table 7-1. Recommended DUT Quantities for Various Radiation Tests

Displacement Damage		**Total Ionizing Dose**		**Ionizing Dose Rate**				**Single-Event Effects**			
unbiased	6	unbiased	5	Operate-through		Survival		Protons		Heavy ions	
controls	2	Q1 (on)	5	Q1 (on)	5		5	30–200 MeV		10–75 MeV-cm^2/mg	
		Q2 (on)	5	Q4 (off)	5		5	(4 energies)		(6 LET values)	
		Q3 ("semi-on")	5	controls	4		4	Q4 (off)	12		18
		Q4 (off)	5					RF	12		18
		RF1	5					controls	3		3
		RF2	5								
		controls	5								
Totals	8		40		14		14		27		39

The number of parts evaluated in characterization testing (and in RLAT) usually is selected to be large enough to apply meaningful statistics to the results, with five parts being a typical minimum number. An example of commonly applied small-sample statistics is sometimes referred to as 90C/99P. This means that there is at least a 90% confidence level that 99% of the parent population will fall within the limits defined by a statistical analysis of the radiation-induced degradation results for a specific device parameter. Application of such statistics involves using a one-sided tolerance factor that depends on the sample size. Guidelines are given in the appendix of MIL-HDBK-814 (1994).

7.7.2 Reference Radiation Environments

To help codify the testing recommendations, the following reference radiation environments are provided. These are typical requirements for a GaN device in a typical system. The test plans below are derived based upon these numbers and may be tailored as necessary for different environments.

- **Displacement Damage Fluence:** equivalent to 2×10^{12} neutrons/cm^2 (1 MeV equivalent)
- **Total Ionizing Dose (TID) at EOL:** 500 krad
- **Ionizing Dose Rate**

- survival to 1×10^{12} rads/sec (peak), 30 ns pulsewidth FWHM (full width, half maximum), recovery after 1 sec
- operate-through 5×10^{9} rads/sec, 1 μsec pulsewidth FWHM, recovery after 1 μsec

- **Heavy-Ion Effects**

  - no performance degradation under exposure to ions with a fluence of 10^{7} ions/cm^2 having LET values up to 75 MeV-cm^2/mg (GaN)
  - no performance degradation under exposure to protons with energy in the range 50–200 MeV with fluence up to 10^{11} p/cm^2
  - no burnout or catastrophic failure

Depending upon the orbit and whether there is a manmade radiation environment, these radiation levels and requirements could be quite different for any given system. The following example test plan outlines have been designed with this reference radiation environment in mind. Tailoring of these plans to the actual requirement is highly recommended.

7.7.3 Displacement Damage Test Plan Outline

Displacement damage (DD) occurs from the proton space radiation environment, or with neutrons from a manmade radiation environment. To simulate these environments in the laboratory, either protons or neutrons may be employed, both capable of producing displacement damage effects. Proton testing is not recommended for devices that are also sensitive to TID effects, since TID and DD effects are difficult to deconvolve. It is recommended here that a nuclear reactor radiation source be employed and that the procedures be followed as in MIL-STD-883K, Method 1017.3 (2015), and in MIL-STD-750-1A, Method 1017.1 (2016).

- **Radiation Source:** Nuclear reactor (preferred) or proton cyclotron source

- **DUT Quantity:** 8 typical

  - includes 2 controls

- **Irradiation Test Condition:** unbiased

- **Procedure**

  - Precharacterize all devices per Sections 3.5 and 3.6.
  - With devices protected from ESD, perform irradiations passively to 5×10^{11} neutrons/cm^2 (1 MeV equivalent) or 25% of the required fluence.
  - Recharacterize per Section 3.3.1.
  - Repeat the previous two steps on the same five samples, with cumulative levels of 1×10^{12}, 2×10^{12}, 5×10^{12}, and 1×10^{13} neutrons/cm^2 (1 MeV equivalent). The final fluence should represent 5× the required fluence.
  - Analyze data based upon failure criteria established for the application. Typical metrics are:
    - threshold voltage changes
    - drain on-resistance R_{Don} increases
    - saturated output power degradations
    - small-signal gain degradations

- transconductance degradations

- **Caveats**

  - The neutron spectrum must be known in order to compute the equivalent monoenergetic (1 MeV) neutron fluence.
  - Depending upon the packaging materials for the GaN devices, they may retain some radioactivity following each exposure, requiring sufficient "cool down" time for personnel safety.
  - Total ionizing dose (or ionizing energy loss, IEL) supplied during the neutron irradiations should be taken into account.
  - If proton testing is employed for DD testing, DD dose should be expressed in units of absorbed dose (MeV/g) or preferably equivalent neutron fluence (neutrons/cm2).

7.7.4 Total Ionizing Dose Test Plan Outline

Total ionizing dose (TID) results from the natural radiation environment consisting of the electron and proton Van Allen belts and manmade radiation or enhanced radiation belts. To avoid dose enhancement effects, a Co-60 source (with gamma-ray energies of 1.17 and 1.33 MeV) is recommended, as are procedures as in MIL-STD-883K, Method 1019.9 (2015), and in MIL-STD-750-1A, Method 1019.5 (2016).

- **Radiation Source:** Co-60 source with Pb/Al container

- **DUT Quantity:** 40 typical, for various irradiation conditions as below

  - Includes 5 controls

- **Irradiation Test Conditions**

  - unbiased 5 DUTs
  - Q1 (on) 5 DUTs
  - Q2 (on) 5 DUTs
  - Q3 ("semi-on") 5 DUTs
  - Q4 (off) 5 DUTs
  - RF1 5 DUTs
  - RF2 5 DUTs
  - Notes:
    - Conditions Q1–Q4 refer to Figure 3-1.
    - Conditions RF1 & RF2 are RF operating conditions tailored for the application, for example, at two different saturated output powers, at two different frequencies, etc.
  - Recommended dose rate is 50 to 300 rads/sec, per Condition A, (see para. 3.6 of MIL-STD-883, Method 1019.9, 2015).

- **Procedure**

  - Precharacterize all devices per Sections 3.5 and 3.6.
  - With devices biased in the appropriate test fixture, perform irradiations for each bias condition to 50 krads or 10% of the required dose.

- Recharacterize per Sections 3.5 and 3.6.
- Repeat the previous two steps on the same samples with cumulative levels of 100, 200, 500, 1M, and 2.5M rad. The final dose should represent 5× the required dose.
- Analyze data based upon failure criteria established for the application. Typical metrics are:
  - threshold voltage changes
  - drain on-resistance R_{Don} increases
  - saturated output power degradations
  - small-signal gain degradations
  - transconductance degradations

- **Caveats**

  - Special test fixturing for the appropriate biasing or RF operation must be provided.
  - The ancillary test fixture/biasing circuitry must be located outside the Co-60 source or be shown to be unaffected by the total dose.
  - While in-flux measurements are not required, in-situ pre-post characterizations (without the need to remove the DUTs from the irradiation fixturing) is desirable to minimize handling errors.
  - ELDRS (enhanced low dose rate sensitivity) has not been found to date in GaN HEMT devices, so low dose rate testing is not necessarily recommended.
  - Testing with dose rates lower than the recommended 50 rads/sec do not invalidate the results.

7.7.5 Ionizing Dose Rate (Survival) Test Plan Outline

Certain manmade environments provide a short-pulsed radiation effect, typically gamma rays. Flash xray machines simulate these environments, and procedures for testing electronic devices can be found in MIL-STD-883K, Methods 1020.1, 2021.3, and 1023.3 (2015), in MIL-STD750-1A, Method 1080.1 (2016), in ASTM F1893-11 (2011) and in ASTM F1262M-14 (2014).

- **Radiation Source: Flash xray (FXR) machine**

  - xray photon mode
  - 2 MeV or greater charging voltage
  - Pulsewidth 10–50 nsec

- **DUT Quantity:** 14 typical, for two irradiations conditions as below:

  - includes 4 controls

- **Irradiation Test Condition**

  - Q1 (on) 5 DUTs
  - Q4 (off) 5 DUTs
    - Note: conditions Q1 and Q4 refer to Figure 3-1.

- **Procedure**

  - Precharacterize all devices per Sections 3.5 and 3.6.

- With devices biased in an appropriate test fixture, perform single-shot irradiations to 1×10^{11}rads/sec (peak) or 10% or the required dose rate.
  - The test fixture should contain a means of readout showing that the device remains functional (not burned out, shorted, or open) after each shot, i.e., using a post-shot DUT DC current monitor, leakage monitor, etc.
  - It is informative to observe the current or output voltage waveform of the DUT output port, or V_{DD} lines on a storage oscilloscope in realtime for each shot.
- Recharacterize per Sections 3.5 and 3.6.
- Repeat the previous two steps on the same DUT, with dose rate levels of 2×10^{11}, 5×10^{11}, 1×10^{12}, and 2×10^{12} rads/sec (peak). The final dose rate should represent 2× the required value.
  - Note: the total dose per shot should be estimated, and when each DUT accumulates more than 20% of the mission requirement dose, it should be replaced with another.
- Analyze pre/post data based upon failure criteria established for the application. Typical metrics are:
  - threshold voltage changes
  - drain on-resistance R_{Don} increases
  - saturated output power degradations
  - small-signal gain degradations
  - transconductance degradations

- **Caveats**

  - Current limiting resistance in the DUT fixturing should be similar to that in the actual application.
  - The radiation pulsewidth may be 10 ns – 50 ns, usually facility dependent.
  - The fixture components shall be shielded or otherwise prevented from producing responses that interfere with observation of the DUT response.
  - It is recommended that the base noise response be observed without a DUT, or with a 50 Ω resistor substituting the DUT.
  - The success criteria are to observe no DUT burnout, with recovery after 1 sec.

7.7.6 Ionizing Dose Rate (Operate-Through) Test Plan Outline

Certain manmade environments provide a lower-intensity, pulsed-radiation effect, typically gamma rays, and xrays. Devices may be required to operate through this environment, with rapid recovery. Procedures for operate-through or upset testing can be found in MIL-STD-883K, Methods 1020.1, 1021.3, and 1023.3 (2015), in ASTM F1262M-14 (2014), and in Aerospace TOR-2006(8583)-5236 (Robertson, 2013).

- **Radiation Source:** electron LINAC

  - Electron energy > 10 MeV
  - Pulsewidth 1–5 μsec
  - Operation in single-shot mode or with PRF less than 10 pulses per second

- **DUT Quantity:** 14 typical, for two irradiations conditions as below:

  - Includes 4 controls

- **Irradiation Test Condition**

  - Q1 (on) 5 DUTs
  - Q4 (off) 5 DUTs
    - Note: Conditions Q1 & Q4 refer to Figure 3-1.

- **Procedure**

  - With devices biased in an appropriate test fixture, capable of readout of DUT output, perform irradiations with a dose rate 5×10^8 rads/sec (average) or 10% of the required dose rate.
    - Capture the current or output voltage waveform of the DUT output port, or V_{DD} lines.
  - Repeat the previous irradiation step on the same DUT, with dose rate levels of 1×10^9, 2×10^9, 5×10^9, and 1×10^{10} rads/sec (average). The final dose rate should represent 2× the required value.
    - Note: the total dose accumulated should be estimated, and when each DUT accumulates more than 20% of the mission requirement dose, it should be replaced with another.

- **Caveats**

  - An appropriate amount of power supply bypassing or stiffening with bypass capacitors is recommended, especially since it is usually not practical to place a power supply near the beam.
  - Any current limiting resistance in the DUT fixturing should be similar to that in the actual application.
  - The electron beam may be collimated so as to expose only the DUT and not the ancillary portions of the test fixture.
  - It is recommended that the base noise response be observed without a DUT or with a 50 Ω resistor substituting the DUT.
  - The success criteria are that the DUT recovers to its pre-pulse electrical condition within 1 μsec or a time as required by the mission.
  - Extensive pre- and post-characterizations are optional.
  - A LINAC beam energy of > 10 MeV is recommended per MIL-STD-883K, Methods 1020 and 1023. The reason is to minimize lower-energy brehmsstrahlung xray production when the electron beam interacts with the target materials, collimator, etc. The low-energy Brehmsstrahlung xrays have a much higher absorption coefficient via the photoelectric effect as compared to the Compton effect absorption of higher-energy xrays. The low-energy contamination causes dosimetry errors and dose enhancement and should be avoided.
  - When using an electron LINAC, replacement currents in the fixturing and target should be considered. Replacement currents flow from ground or other sources to replace electrons scattered out of the solid materials of target and fixturing.
  - Most electron LINACs operate at L or S band, in pulsed mode with pulsewidths from about 0.5 to 10 μsec. During this pulse, the electrons come in bursts at the LINAC operating frequency. If the DUT is a high-frequency device such as a GaN HEMT, the LINAC frequency may be in-band. This can cause difficulties, oscillations, and anomalies.
  - By the same token, the LINAC electron bursts have peaks with much higher instantaneous dose rate than the dose rate averaged over the entire radiation pulse period. This may create erroneous interpretations if the photocurrent response of the DUT tracks the bursts (McLain, 2018).

7.7.7 Single-Event Proton Test Plan Outline

Earth's trapped radiation belts can impart significant fluxes of protons at various energies, depending upon a satellite orbit. In addition to displacement damage, the protons can sometimes induce single-event effects, such as upset or burnout in GaN HEMTs. A proton cyclotron can provide the necessary fluence to simulate these effects in the laboratory. Procedures for performing proton single-event tests can be found in Buchner (2002), in JEDEC JESD234 (2013), in ESA ESCC-25100 (2014), and in Aerospace TOR-2006(8583)-5236 (Robertson, 2013).

- **Radiation Source:** Proton cyclotron
  - Proton energy E_p = 30 – 200 MeV
- **DUT Quantity:** 27 typical, for 8 irradiations conditions as below:
  - Includes 3 controls
- **Irradiation Test Condition**
  - Q4 (off) 3 DUTs E_p = 30 MeV
  - 3 DUTs E_p = 80 MeV
  - 3 DUTs E_p = 120 MeV
  - 3 DUTs E_p = 200 MeV
  - RF1 3 DUTs E_p = 30 MeV
  - 3 DUTs E_p = 80 MeV
  - 3 DUTs E_p = 120 MeV
  - 3 DUTs E_p = 200 MeV
  - Notes:
    - Condition Q4 refers to Figure 3-1.
    - Condition RF1 is an RF operating conditions tailored for the application, for example, with similar output power, at a typical frequency, etc.
- **Procedure**
  - Precharacterize all devices per Sections 3.5 and 3.6.
  - With a single device biased in an appropriate test fixture, capable of readout of DUT output, supply protons with the energy as listed above to a fluence of 10^{11}p/cm^2 in the Q4 test condition.
    - Capture the current or output voltage waveform of the DUT output port, or V_{DD} lines, checking for burnout, upset, or sudden changes in performance.
  - Repeat the previous irradiation step on the next DUT, with the same fluence and proton energy.
  - Repeat the above for the all four proton energies in conditions Q4.
  - Repeat the above for all four proton energies in condition RF1.

- **Caveats**

  - Protons with energies less than about 30 MeV are shielded by typical satellite exterior shells. In cases where there is less shielding, lower-energy protons should be included in the testing.
  - Proton irradiation provides both displacement damage and total ionizing dose. These should be estimated for each irradiation. If either exceeds about 20% of the mission requirements, then additional DUTs may be required to achieve the total required fluence of 10^{11} p/cm^2.
  - Conversely, if the displacement damage is not large for fluence value, DUTs may be re-used for successively higher proton energy values. In the best case, only three DUTs would be required for all the steps from 30 to 200 MeV.
  - Direct proton cross section is estimated to be $N/10^{11}$ cm^2 if there are N events, such as upsets by the time the fluence of 1×10^{11} p/cm^2 is reached.
  - Direct proton cross section is bounded to be below $(N\chi^2_{N+2,C})/2\times10^{11}$ cm^2 with confidence factor C if there are N events by the time the fluence of 1×10^{11} p/cm^2 is reached, where $\chi^2_{N+2,C}$ is the chi-squared distribution with $N+2$ degrees of freedom, and fractile C.
  - Direct proton cross section is bounded to be no greater than $-\ln(1-C)/10^{11}$ cm^2 with confidence factor C if there are no events up to a fluence of 1×10^{11} p/cm^2.
  - If a burnout occurs after fluence ϕ, an estimate of the burnout cross section is $1/\phi$. Burnout cross section estimates should be averaged for the three (or more) DUTs if they occur. Burnout cross section is bounded to be below the chi-square limit as defined above for the three (or more) events, adding the total fluence for all.
  - Burnout may not occur (hopefully); however, gate leakage may increase in certain devices because of the displacement damage.
  - SEDR in MIMCAPs or in the dielectric under field plates in HEMTs can occur due to protons with a small but finite probability. The protons may create fission fragments from adjacent high-Z materials such as Au in packaging or in the Au metallization used on the die. It may be necessary to perform proton SEDR tests with the GaN die mounted in its intended packaging to observe this effect. This may be necessary if a proton-rich radiation environment is specified. It is important to distinguish SEDR failures from failures in the semiconductor regions of HEMTs.
  - HEMTs or MMICs with Si substrates may have a greater tendency to experience burnout than devices with native GaN or SiC substrates.
  - It is recommended that the tests be conducted with a drain voltage 20% higher than the usage voltage in order to provide an overtest margin.
  - The proton energies recommended here have sufficient penetration through typical packaging materials to make it unnecessary to thin the encapsulation or remove lids. In fact it may be preferable to include mission-like packaging to test for the abovementioned SEDR in MIMCAPs due to proton fission reactions.

7.7.8 Single-Event Heavy-Ion Test Plan Outline

Cosmic rays and solar flares are sources of heavy ions in space. These heavy ions are single atomic nuclei stripped of electrons and have very high energies, capable of penetrating electronics. These heavy particles can sometimes induce single-event effects, such as upset or burnout in GaN HEMTs. For an RF/microwave HEMT, events classified as SEUs (single-event upsets) may not be nearly as problematic as SEB (single-event burnout). A heavy-ion cyclotron can provide the necessary fluence to simulate these effects in the laboratory. Procedures for performing heavy-ion single-event tests can be found in MIL-STD-750-1A, Method 1080.1 (2016), in JEDEC JESD57A (2017), in ASTM F1192-11 (2011), in ESA

ESCC-25100 (2014), in Aerospace TOR-2006(8583)-5236 (2013), and in Sandia (Schwank, 2013a and b).

- **Radiation Source:** Heavy Ion Cyclotron
  - Particle energy 5–50 MeV/nucleon dependent upon facility
  - LET values 10–75 MeV-cm^2/mg (GaN)
- **DUT Quantity:** 39 typical, for 12 irradiations, conditions as below:
  - Includes 3 controls
- **Irradiation Test Condition**

–	Q4 (off)	3 DUTs	LET ≈ 10 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 25 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 40 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 50 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 65 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 75 MeV-cm^2/mg (GaN)
–	RF1	3 DUTs	LET ≈ 10 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 25 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 40 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 50 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 65 MeV-cm^2/mg (GaN)
–		3 DUTs	LET ≈ 75 MeV-cm^2/mg (GaN)

  - Notes:
    - Condition Q4 refers to Figure 3-1.
    - Condition RF1 is an RF operating condition tailored for the application, for example, with similar output power, at a typical frequency, etc.
    - For many space robotics missions, testing to a maximum LET of only 40 MeV-cm^2/mg may be sufficient.
- **Procedure**
  - Precharacterize all devices per Sections 3.3 and 3.6.
  - With a single device biased in an appropriate test fixture, capable of readout of DUT output, supply heavy ions with the LET values as listed above to a fluence of 10^7ions/cm^2 in the Q4 test condition.
    - Capture the current or output voltage waveform of the DUT output port, or V_{DD} lines, checking for burnout, upset, or sudden changes in performance.
  - Repeat the previous irradiation step on the next DUT, with the same fluence and LET.
  - Repeat the above for all six LET values in conditions Q4.
  - Repeat the above for all six LET values in conditions RF1. If a test configuration and LET condition can be identified that initiates SEB, repeat that case on a fresh sample varying the angle of incidence.

- **Caveats**

  - Heavy-ion irradiation provides both displacement damage and total ionizing dose. These should be estimated for each irradiation. If either exceeds about 20% of the mission requirements, then additional DUTs may be required to achieve the total required fluence of 10^7 ions/cm^2.
  - Conversely, if the displacement damage is not large for each LET value, DUTs may be re-used for successively higher LET values. In the best case, only three DUTs would be required for all the steps from 10 to 75 MeV-cm^2/mg.
  - Cross section is estimated to be $N/10^7$ cm^2 if there are N events (such as upsets) by the time the fluence of 1×10^7 ions/cm^2 is reached.
  - Cross section is bounded to be below $(N\chi^2_{N+2,C})/2\times10^7$ cm^2 with confidence factor C if there are N events by the time the fluence of 1×10^7 ions/cm^2 is reached, where $\chi^2_{N+2,C}$ is the chi-squared distribution with $N+2$ degrees of freedom, and fractile C.
  - Cross section is bounded to be no greater than $-\ln(1-C)/10^7$ cm^2 with confidence factor C if there are no events up to a fluence of 1×10^7 ions/cm^2.
  - If a burnout occurs after fluence ϕ, an estimate of the burnout cross section is $1/\phi$. Burnout cross section estimates should be averaged for three (or more) DUTs if they occur. Burnout cross section is bounded to be below the chi-squared limit as defined above for the three (or more) events, adding the total fluence for all.
  - It is recommended to start with the higher LET values in the list and proceed downward in LET from there. This minimizes the total dose accrued.
  - Gate leakage may increase in certain devices because of the displacement damage.
  - HEMTs or MMICs with Si substrates may have a greater tendency to experience burnout than devices with native GaN or SiC substrates.
  - It is usually desirable to locate the Bragg peak well beyond the sensitive depth of interest. The sensitive depth is often assumed to be the thickness of the AlGaN barrier plus the GaN buffer. The sensitive depth may, however, include the substrate, necessitating higher-energy ions to push the Bragg peak out. (See Appendix G, Section G.5.)
  - A strong angular dependence of SEB in GaN HEMT devices may be found. This also suggests the sensitive volume may go beyond the 2DEG region and include the buffer and substrate.
  - It is recommended that the tests be conducted with a drain voltage 20% higher than the usage voltage in order to provide some overtest margin. If burnout is observed, the voltage on the next sample should be lowered stepwise until no burnout is observed. This establishes the threshold voltage for burnout.
  - A success criterion is typically that there are no burnouts or decreases in performance to a fluence of 10^7 ions/cm^2 up to a maximum LET of 75 MeV-cm^2/mg. A different maximum LET success criterion value may be needed, depending upon the radiation environment and mission.
  - SEDR in MIMCAPs or in the dielectric under field plates in HEMTs are always possible with heavy ions having higher LETs. It is important to distinguish SEDR failures from failures in the semiconductor regions of HEMTs.
  - Galactic cosmic rays can have energies up to the GeV range, while the typical cyclotron is limited to much lower energies. Therefore, to allow the ions to penetrate the active device area, the package lids, packaging material, overlayers, etc., usually must be removed.
  - It is recommended that the SRIM™ program (Ziegler, 2008) be utilized in order to estimate the LET at the sensitive depth. Overlayers and their effect on the LET should be taken into account. The LET for GaN or AlGaN is typically about 80% that for Si. The LET for SiC is closer to the LET value for Si. (See Appendix G.5.)

8. Open Issues and Recommended Work

At the time of this writing, there are a few loose ends and open issues regarding GaN HEMT space qualification. More work is needed in a number of areas. What follows is a short list of items in this category that deserve further investigation.

1. In this guideline (Section 3.1) the assertion has been made that DC-only accelerated testing will be sufficient to qualify a GaN HEMT transistor or MMIC for a wide variety of applications. This is motivated by the difficulty and cost associated with a complete multi-temperature multi-loadline RF driven set of accelerated tests. Four DC Q-points have been recommended (see Figure 3-1). To complete the picture, it is recommended that the DC testing be followed up with a relatively smaller scale RFALT (RF accelerated lifetest) and a more extended-duration TLYF test (test like you fly). The validity of this approach has been based upon some preliminary data. However, the assumptions underpinning this recommendation need further verification. The approach may be overly conservative. What is needed is a more complete comparison between the lifetimes at the accelerated DC conditions of Figure 3-3 versus stress under an example RF loadline. The problem of correlating the DC to RF conditions is difficult because the RF loadline depends upon much more than simply the device itself. The shape of the RF loadline (generating the electrical stress) depends upon the loading impedance, output match or VSWR, distortion effects, and compression levels as much as it does the RF device itself. The RF and microwave circuit design space is very large compared to the DC test space. This is a challenging question and deserves more investigation.

2. Along similar lines, the presence of a large-signal RF in a transistor has been postulated to cause different reliability effects as compared to a DC condition. In other works, stressing at a DC Q-point where the voltage and current are made equal to the RF peak or RMS voltage and current has been suggested to produce different reliability effects. The presence of the RF signal could give different stresses and degradations as compared to DC. In this hypothesis, DC testing can never serve as a surrogate for RF testing. This has been reported anecdotally in the execution of SEB testing, where RF is needed to generate a burnout where a DC level does not. More work needs to be accomplished to verify this effect in more routine accelerated testing for reliability.

3. A dynamic current voltage analyzer (DIVA) or pulsed IV (PIV) system has been recommended in this guideline as one way to characterize the traps in a GaN HEMT. In these methods the traps-filled or trap-empty IV curves indicate the existence and effect of the traps. The traps may increase in density upon stressing or radiation and can be tracked by changes in the dynamic IV curves. This method is proposed here toward a standard way of characterizing the traps. It is not as thorough as other methods, such as DLTS (deep-level transient spectroscopy) or DLOS (deep-level optical spectroscopy), since the trap energy levels, cross sections, and relaxation times are not explicitly measured. However, the direct effect of these traps on IV curves is readily seen with equipment that is readily available. The trap effects can be observed on production devices rather than special test structures. More work needs to be done toward standardizing this approach, including calculating the pulse durations needed and the traps-empty and traps-full Q-point positions (QE and QF), and interpreting the results.

4. It is claimed that GaN HEMTs and MMICs are “intrinsically” radiation hard. This is mostly because of the high TID (total ionizing dose) and DD (displacement damage) levels needed to cause changes to DC and small-signal characteristics. Little work has been done to characterize the effect on the trapping phenomena. More work needs to be accomplished to expand the radiation effects on trapping in GaN HEMTs.

5. The moisture levels inside hermetic packages have been mentioned in this guideline as a possible issue of concern. For example, moisture can induce corrosion at the gate of a HEMT. It can react with GaN to generate NH_3 (ammonia) gas. It is unknown currently whether the traditional acceptable quantity of water vapor inside a hermetic module of 5,000 ppmV is safe and compatible with GaN devices for a long mission. More work needs to be done to quantify the levels of ammonia that will be generated and the degree of harm that it may engender on the contents inside the microwave module, including the GaN device itself.

6. In this guideline the concept of the critical voltage V_{crit} has been discussed. Above V_{crit}, the device characteristics degrade due to the drain voltage or electric field effects rather than just the thermal effect. The device reliability takes on a TDDB-like (time-dependent dielectric breakdown) character. With voltages above V_{crit}, new traps are believed to be generated due to increased piezoelectric strain. Simple reliability models have been proposed (Section 3.2) to include the effect of voltage on device lifetime. These models do not yet have any clear connection to physical mechanisms. Their saving grace seems that they describe the phenomena fairly well and can be fitted to data. More work needs to be done to solidify these models and relate them to device physics. It is unknown whether all GaN HEMTs suffer from the voltage or TDDB-like effect or whether the effect can be engineered away. On the other hand, the field-dependent material properties of AlGaN and GaN may be unavoidable. The presence of field plates of various kinds may improve or eliminate the V_{crit} effect. Device design and geometry could have a large impact on the voltage-dependent lifetime. These are open questions at this time.

7. Material quality continues to improve in the GaN HEMT technology. The present dislocation density of starting material of approximately 10^6 defects/cm^2 may continue to decrease. An improved material quality could lead to longer carrier lifetimes and fewer traps, lessening the current collapse effect. These would be major improvements. Improved material quality could also have certain disadvantages, such as an increased SEE transient response or more TID sensitivity. Where (and whether) this tradeoff exists is presently unknown.

8. To map the SOA (safe operating area) in the IV plane of a GaN HEMT, destructive tests are advocated in this guideline (Sections 2.1–2.3). There may be a better way using high-speed transmission line pulsers (TLPs). This is test equipment originally intended for CDM (charged device model) ESD (electrostatic discharge) testing. Some of the rise times and pulse durations of the available equipment are compatible with speeds reported for GaN HEMT burnout. The idea behind the TLP is that the device can be pulsed rapidly, and the snapback, or negative resistance regime, entered readily. If the event is kept sufficiently short, it is nondestructive. With precise pulse control, it may be possible to observe the snapback effect repeatedly without actually damaging the device. If this were possible, the SOA could be mapped out fully with just one sample. This would be great improvement over the need to destroy multiple samples to observe the SOA. This is a fertile area for more work.

9. Power GaN HEMT devices called “enhancement mode HEMTs” have been developed and are now available. They utilize different gate materials, such as a p-type GaN semiconductor to shift the threshold voltage to a positive value as compared to a conventional Schottky gate HEMT. In the future is it is possible that this idea will be migrated to RF and microwave HEMTs. The failure mechanisms of these devices may well be different than conventional HEMTs. This has not yet been much explored.

10. Similarly, MIS-HEMTs (metal-insulator-semiconductor HEMTs) have also been proposed for both power and RF/microwave applications. A MIS-HEMT is a field effect device combined with a 2DEG (two-dimensional electron gas) sheet conduction. It does not possess a Schottky barrier

and is not addressed in this guideline. Failure mechanisms in MIS-HEMTs may include all those described in this guideline, plus some new ones. The presence of the insulated gate poses a new set of reliability and radiation concerns. More work needs to be done to understand the long-term reliability failure mechanisms of a MIS-HEMT, the methods to accelerate them in the laboratory, and their radiation effects. Perhaps in the future it will be necessary to expand this guideline to include MIS-MEMTs or to write a new guideline.

11. Deratings in this guideline have been recommended such that the lower statistical limit of the breakdown voltage (at the right side of the SOA) is at least 2× to 3× higher than the rated safe maximum drain-source voltage $V_{DSsafe.max}$. Other reliability or SEB constraints may need to be added to this derating and have been discussed. Above the critical voltage V_{crit}, there is a TDDB-like (time-dependent dielectric breakdown) effect that worsens for higher and higher voltages. More work needs to be done to justify the 2× to 3× derating.

12. A standard way to specify maximum ratings for GaN HEMTs and MMICs has been proposed in Tables D-1 and D-2, respectively. It is hoped that the users and providers of space-grade, high-reliability RF and microwave GaN HEMTs and MMICs will consider adopting this standard. The types of ratings and the degree of conservatism built in to these ratings is an open question. As the GaN technology becomes more established, with more SOA and reliability data available, a relaxation of the level of this conservatism could be warranted.

13. MIMCAPs may drive the long-term reliability of a large MMIC. The MIMCAP reliability model proposed here (Appendix F) is one based upon Frenkel-Poole conduction followed by "exhaustion." Charge-to-breakdown has been used as the criterion for failure. The current conduction properties of insulators are complex and dependent on the fabrication materials and process. Other models have been used to model the MIMCAP reliability. Some are not influenced by the current density or charge but rather the electric field. Others are phenomenological. More work is needed to understand the nature of the breakdown voltages for defects in MIMCAPs.

14. Hydrogen sensitivity has been a traditional issue with many GaAs pHEMTs. For GaN HEMTs there has not been much reported about this issue. However, the conditions seem ripe for the same phenomena—molecular hydrogen diffusing through passivation, catalyzation into atomic hydrogen by Pt, Pd or other gate metals, hydridization of the gate metal inducing a volume change, inducing a mechanical strain, then causing a piezoelectric threshold voltage shift. The threshold voltage shift cannot be accommodated with passive bias networks, and the device debiases and loses gain and output power. This same set of events seems to be likely in a GaN HEMT. This should be verified and tested with multiple hydrogen levels and temperatures just as has been the case for GaAs HEMTs. This is work that remains to be done.

15. In similar fashion, the buildup of ammonia has been a concern in the presence of moisture in GaN HEMTs. This potential issue should be explored more thoroughly by performing experiments on GaN device sensitivity to low levels of ammonia. Some advanced ceramics—such as AlN—are being proposed as housing materials for GaN HEMTs for operation at high temperature. The levels of ammonia that may be produced inside an AlN package need better quantification. Even if hermetic packages are sealed conforming with leak rates that meet traditional requirements, small intrusions of air and moisture still occur over long periods. If moisture builds up and reacts with the AlN to produce ammonia, that would be undesirable. This issue has not been thoroughly investigated to date.

16. In performing single-event effects testing using protons versus heavy ions (excepting the accompanying total ionizing dose or displacement damage effects), an open question exists.

Firstly, the use of protons generally does not require thinning or de-lidding the packages since the ranges of the protons can usually penetrate these materials easily. Therefore protons make for a simpler test protocol. But the proton LET may not be sufficient to cause an SEE unless nuclear reactions occur. For example, the creation of Ge energetic ions (Ga + proton = Ge) is the worst case. If heavy ion tests are performed with Ge at the typical available energies at cyclotron facilities and no events are found, then it seems likely that proton testing would not be useful. The necessary experiment has not yet been performed, and the issue remains open. On the other hand, fission reactions from protons onto high-Z packaging materials and/or metallization adjacent to MIMCAPs may necessitate proton testing of a fully packaged device for SEDR (single-event dielectric rupture). This, too, is an open question.

17. Similarly, in performing single-event testing using only heavy ions, it is still unknown whether there is a species dependence. For Si MOSFETs, it has been found that ions of different species but identical LETs have different SEB and SEDR responses. This is believed to be related to the difference in the spreads of the ionization tracks or columns in the target Si material. It is unknown whether a similar difference is important in GaN HEMTs. There may be other differences to consider, such as the different substrates used for GaN HEMTs (SiC, Si, sapphire, etc.). The possibility of a species dependence on SEB in GaN HEMTs and MMICs has not been investigated. Further, the angular dependence of SEB can be observed in some GaN HEMTs but not in others. This indicates that there are differences in the nature of the sensitive volumes between devices. The role of the substrate in the SEB effect is likely at play. This is an area that deserves more investigation. It is also unknown whether a relationship exists between the LET and the SEB burnout voltage in a GaN HEMT like the Titus-Wheatley empirical formula for Si power MOSFETs. If so, this would be a very valuable tool. Many more tests would be required to definitize this. At this time, the avoidance of burnout can be handled only with possibly an excess conservatism in voltage derating. More work is needed in this area.

This guideline is intended to aid the space community in qualifying GaN HEMT–based RF and microwave electronics and payloads for space. In the future, it is hoped that the guidelines can evolve and improve as the technology matures. Suggestions for future revisions and additions are welcome. An additional effort could be devoted towards maintaining and updating this guideline. The guidelines are mainly intended for qualification of GaN RF/microwave HEMTs and MMICs for ultrahigh-reliability Class A and B missions. There are many other space missions with less stringent reliability requirements, shorter mission durations, and lower levels of aging. For these missions, too, it is hoped that some of these guidelines are applicable. A future activity might be to investigate the relaxation of requirements called out herein. This would require much justification, rationale, and real data and would be a worthwhile future task.

9. Fifty Qualification Questions to Ask Your GaN HEMT or MMIC Supplier

The following list of questions might be helpful when posed to a contractor or supplier of GaN HEMTs or GaN MMICs. Answers provided may help underscore the need to perform additional tests or further assess the reliability of a GaN HEMT process or product. These questions are based upon the guidelines proposed in this document. Not all the questions necessarily directly apply to a particular device, a certain mission, or an individual need. For example, phase noise is not a requirement for some missions, but critical for others.

The questions have been developed for the benefit of the procurer or user of GaN HEMTs or MMIC parts as they discuss technical requirements with their customers and then translate those requirements into reliability specifications for their suppliers or reliability expectations for the program. It is hoped that the following questions are worthwhile and complete:

1. Have reliability tests been performed at multiple temperatures and with multiple DC bias points (Q-points)? Do the multiple DC bias points bound the actual loadline for the anticipated usage?

2. Which one of the DC Q-points provides the lowest MTF (median time to fail) at the mission usage conditions?

3. Has an RF-driven accelerated reliability test been performed?

4. Do DC tests correlate with RF-driven tests?

5. Is there a dominant failure mechanism? If so, what is it? If not, how many competing mechanisms exist? How do they change in importance with respect to each other as the conditions (temperature, bias, RF drive, age) are changed?

6. How have the channel temperatures in accelerated tests and in the mission hardware been determined? How accurate are they? Has an error or sensitivity analysis been performed for the effect of channel temperature uncertainty on reliability predictions?

7. Does gate metal migrate or disappear?

8. Has the reliability (FITs) been estimated for the mission?

9. Has a TLYF (test like you fly) test been performed over at least 15% of the mission duration?

10. Has a “sneak” lower temperature failure mechanism been uncovered?

11. Does long-term degradation have a voltage dependence, and has a critical voltage V_{crit} been determined for the process? V_{crit} is the voltage above which the time-dependent, voltage-driven failure mode manifests. What is the form of the model for the voltage-dependent degradation (if it exists)?

12. Has an SOA (safe operating area) been determined for the drain-source IV plane? DC or pulsed?

13. Is the maximum safe drain voltage specified? Is it at least 2× to 3× lower that the minimum catastrophic breakdown voltage 3σ limit?

14. Has the maximum safe drain current been specified? Is it at least 2× lower than the minimum failure current 3σ limit?

15. Has an SOA been determined for the gate-source IV plane? DC or pulsed?

16. Has the maximum reverse safe gate voltage been specified? Is it at least 2× to 3× less negative than the least negative catastrophic breakdown voltage 3σ limit?

17. Has the maximum safe forward gate current been specified? Is it at least 2× lower than the minimum failure current 3σ limit?

18. Has RF survivability been shown to meet the mission requirements?

19. Does "current collapse" occur if a pulsed RF usage condition is intended? Has it been characterized at EOL?

20. Does pulse-to-pulse instability or distortion occur? Is it adequately characterized for the mission and at EOL?

21. Does the circuit or MMIC experience gate debiasing when overdriven to levels of interest? If so, has the recovery time from the overdrive been shown to be satisfactory for the mission?

22. Has the threshold voltage stability at EOL been determined?

23. Have the trap time constants or pulsed IV characteristics been measured? Are they affected by radiation? Do they change at EOL?

24. Has low-frequency noise ($1/f^n$ noise) or phase noise been measured? Is it affected by radiation? Does it change at EOL?

25. Has the MIMCAP defect density been characterized using process monitoring using a ramp breakdown test over many samples? Are running statistics on the DOAs (dead on arrivals or shorts) and extrinsics (low ramp breakdown voltages) kept?

26. Has the MIMCAP reliability been determined for the mission based upon the measured defect density after all screening, burn-in, integration testing, etc., are accounted for?

27. Has a MIMCAP voltage screen been implemented?

28. Have rules for the design of electromigration maximum current density been established for the process? Have they been followed in the circuit or MMIC, particularly at the gate feed(s)? Do the rules support the mission reliability requirement at the mission temperature and duration?

29. Has the rule about the design of the thin film resistor (TFR) maximum current density vs. size been established? Has it been followed in the circuit or MMIC for all resistors? Does the design rule support the mission reliability requirement at the mission temperature and duration? Has TFR temperature rise under worst-case power been verified using a thermal IR imager or similar technique?

30. Has the backside via reliability been characterized? Does it meet mission requirements?

31. Has the effect of total ionizing dose (TID) on device performance been characterized? Does the result support the mission requirements? Does TID affect dynamic trap-related performance such as pulse-to-pulse instability or distortion, noise, and current collapse at EOL?

32. Does the radiation-produced displacement damage (DD) affect device performance? Does the result support the mission requirements? Does DD affect dynamic trap-related performance such as pulse-to-pulse instability or distortion, noise, and current collapse at EOL?

33. Have dose rate–induced transient currents been measured? Have the mission performance goals for transient effects been met?

34. Have proton and heavy ion tests been performed? Does the HEMT or MMIC experience SEB (single-event burnout)? Have a threshold LET and saturated cross section for SEB been determined? Have the SEB threshold and saturated cross section been measured over a range of voltages below the specified $V_{DSmax.safe}$?

35. Has the GaN device itself been tested in a proton beam for fission-induced SEDR (single-event dielectric rupture) of MIMCAPs or field-plates? Has it been tested for proton SEDR in its intended packaging, especially for packages or modules that contain Au, Au plating, or other high-Z materials?

36. Have a burn-in procedure and post burn-in accept/reject criteria for HEMTs and MMICs been established? What fallout occurs as a result of burn-in? What changes in device characteristics occur after burn-in? Do the changes remain stable after the burn-in?

37. Has the defect density for the gates been determined on unscreened devices using a ramped voltage on an adequate sample size? Are the defects effectively screened by the burn-in procedure or other screens? Has the "consumer's risk" been determined?

38. Has the ESD sensitivity of the HEMT or MMIC been established?

39. Has bondwire reliability been assessed with multiple groups of bonds exposed to temperature bakes and measured for bondpull strength?

40. Has backside metal integrity been assessed?

41. Has a bake test been performed on airbridges?

42. Has hydrogen sensitivity of the HEMT or MMIC been established? Is there a hydrogen getter needed in hermetic modules or packages?

43. Has moisture sensitivity of the HEMT or MMIC been established? Does moisture induce electrochemical reactions and pitting in the region near the gate? Does the moisture-induced degradation rate meet the mission reliability goals?

44. In the presence of moisture, does ammonia build up in a hermetic module with this HEMT or MMIC? Is the GaN device itself sensitive to ammonia? Do other items in the hermetic module or package have an ammonia sensitivity?

45. Does the GaN HEMT or MMIC have an air or oxygen sensitivity?

46. Has an off-state bias test or HTRB (high-temperature reverse bias) screen been implemented for HEMTs or MMICs? Does more than 2% of product fail this screen? Is the screen effective in removing product that would have unacceptably low breakdown voltage in off-state burnout or SOA tests?

47. Has a test for LFOs (low-frequency oscillations) been performed?

48. Has the device in its package been temperature cycled to failure? Have the results been analyzed for compliance with mission requirements, using the Coffin Manson approach?

49. Has the device in its package been power cycled (on/off)? Are the results compatible with the mission?

50. Is the device in its packaging and configuration in the system at risk for multipaction? How is this mitigated?

Appendix A. GaN HEMT Technology Qual Checklist

The following table summarizes all the various qualification tests that have been proposed in this guideline. It serves as a checklist to aid in tailoring the particular set of tests that may be needed for any proposed mission. Not all qualification tests will be required for every mission. The ordering of the tests roughly matches the order of their appearance in the main document.

A preliminary version of this table was generated by Andy Moor, Ron Hardesty, and Randall Lewis of Northrop Grumman Corp., who are gratefully acknowledged.

Test Description	Purpose	Sample Size	# of sample lots	Environment / Conditions	Failure Criteria
2.1 DC Drain-Source SOA (destructive)	Capture empirical device data; drive samples to failure in controlled manner to establish DC IV destruct boundaries	100	3	250 °C (baseplate); stepped drain voltage	Sudden drain current increase
2.1.1 Pulsed Drain-Source SOA (destructive)	Capture empirical device data; drive samples to failure in controlled manner to establish pulsed IV destruct boundaries	100	3	250 °C (baseplate); pulsed drain voltage	Sudden drain current increase
2.2 DC Off-state Burnout (destructive)	Capture empirical device data; drive samples to failure in controlled manner to establish VDS off-state destruct value	50	3	250 °C; (baseplate) stepped drain voltage; DC Gate voltage at full pinchoff	Device failure
2.3 DC Gate Damage Threshold (destructive)	Capture empirical device data; drive samples to failure in controlled manner to establish V_G damage threshold	24 forward, 24 reverse polarity	3	>250 °C (baseplate); stepped drain voltage, nonoperational and operational condition	Immediate damage
2.4 Off-State High-Voltage Screen Demonstration	Demonstrate that the chosen HV screen procedure is consistent with ratings & SOA; weed out defective HEMTs, MIMCAPs	100% of product	all	150 °C, maximum rated drain and gate voltages or higher, 1 sec. min.	>2% of product has in-situ leakage > than the developed max value
2.5 ESD Tests (destructive)	Capture empirical device data demonstrating susceptibility to induced ESD events using the Human Body Model (HBM)	HEMTs: 40 MMICs: pin count dependent	3	Room ambient; MIL-STD-883, Method 3015.9; increase exposure voltage by defined steps until failure	Device failure
	Capture empirical device data demonstrating susceptibility to induced ESD events using the charged device model (CDM)	HEMTs: 20 MMICs: pin count dependent	3	Room ambient; JEDEC JESD-22-C101F; increase exposure voltage by defined steps until failure	Device failure
2.6 RF Burnout/ Survivability (destructive)	Capture empirical device data establishing the damage threshold for high-power RF drive (destructive)	12	3	Room ambient or max. usage temperature; RF peak output voltage ≥ $V_{DSmax.safe}$. RF pulse train for 1 minute with 10 μs pulses, 1% duty cycle, RF input level stepped up in 1 dB increments	Per Section 3.7
2.7 Temperature Cycling (destructive)	Establish thermal cycle durability using Coffin-Manson with q = 4 (CDI = 0.25) (destructive)	75	3	JEDEC JESD22-A104D, -55C to +200C, (JEDEC JESD47-I, Annex A) [Use of Coffin-Manson approach can reduce the # of cycles by ~100×]	Per Section 3.7
2.8 Power Cycling	Establish power cycling capability with voltage-inducing piezoelectric strain, and cyclic internal dissipation	36	3	150 °C (baseplate) or max. usage temperature; DC power cycled at bias cond. "C" of Figure 2-1; period 2 min; 50% duty cycle, 168 hr	Per Section 3.7

Test Description	Purpose	Sample Size	# of sample lots	Environment / Conditions	Failure Criteria
3.3 DC HEMT combined TALT & VALT (destructive) **(Temperature Accelerated Lifetest & Voltage Accelerated Lifetest)**	Full set of DC-accelerated tests covering four Q-points:	TOTAL 400 typ 200 min	3	Combined voltage and temperature acceleration test scheme per Figure 3-3	
	• Q1: traditional power dissipating condition central to IV plane	60 typ 30 min	3	•Select 3 channel temperatures. •Select $V_{DS} < V_{crit}$	Per Section 3.7
	• Q2: high-current/low-voltage condition	60 typ 30 min	3	•Select 3 channel temperatures. •Select $I_D \geq I_{Dmax.safe}$ •Select low V_{DS}	Per Section 3.7
	• Q3: low-current/high-voltage condition ("semi-on")	140 typ 70 min (fewer if no V_{crit})	3	•Select combined temperatures/voltages per Figure 3-3, includes V-T interaction effects	Per Section 3.7
	• Q4: off state (zero power dissipation)	140 typ 70 min (fewer if no V_{crit})	3	•Select combined temperatures/voltages per Figure 3-3, includes V-T interaction effects •$T_{channel} = T_{baseplate}$	Per Section 3.7
3.4 DC HEMT TSST (Temperature Step-Stress test)	•Establish temperatures for future TALT •Distinguish failure mechanisms	8 min (2 DUTs × 4 Q-points)	2	•start at 150 °C (channel •T stepped by 5 °C – 25 °C every 18 to 24 hrs. • $T_{baseplate}$ adjustments for const. $T_{channel}$	Per section 3.7
3.4 DC HEMT VSST (Voltage Step Stress Test)	•Determine V_{crit} to support other accelerated tests •Distinguish failure mechanisms	5	5	•V_{DS} stepped by IV every 18 to 24 hrs. •Semi-on condition (Q3) •150 °C (baseplate) •$T_{baseplate}$ adjustments for const. $T_{channel}$	Per section 3.7
3.8 Alternate Approach-Signature Parameters (SPs)	Alternate method to avoid RF interim measurements—DC stress of DUT with interim meas. of SPs TBD; but requires RF-driven stress for correlation; 2TLT or 3TLT at 3-4 Q points followed by DC-only measurements once failure mechanisms are associated with SPs	Q1: 60 20 min	3	•Select 3 (2 min) channel temperatures •Select $V_{DS} < V_{crit}$	Per section 3.7
		Q2: 60 20 min		•Select 3 (2 min.) channel temperatures. •Select $I_D \geq I_{Dmax.safe}$ •Select low V_{DS}	
		Q3: 60 20 min		•Select 3 (2 min.) channel temperatures •Select $V_{DS} > V_{crit}$ •Semi-on state	
		Q4: 60 20 min		•Select 3 (2 min.) channel temperatures •Select $V_{DS} > V_{crit}$ •Off state	
		RF: 60 20 min		•Select 3 (2 min) channel temperatures •Select accelerated RF stress condition	
	TOTAL: 300 (100 min)				

Test Description	Purpose	Sample Size	# of sample lots	Environment / Conditions	Failure Criteria
3.10 RF-driven Accelerated Lifetest (RFALT)	Corroboration of failure mechanisms; test more closely simulates usage. Captures data in a more relevant use-case environment	20 (10 min)	3	•Select 2 (1 min) channel temperatures elevated above usage temperature •reasonable overdrive condition exceeding usage •Compression level of usage or greater •Pulsed or CW drive should match the application •Elevated V_{DS} but peak RF $V_{DS} < V_{DSabs.max}$.	Per Section 3.7
3.12 Long-Term Test (Test Like You Fly) TLYF	Demonstration of real operation with only mild acceleration of stressing conditions; eliminates possibility of "sneak" low activation energy failure modes	30 devices	3	•15% of mission duration •RF drive and bias voltages should be usage values •temperature must be managed close to anticipated usage profile	Per Section 3.7 –or– Select interim measurements and failure criteria to match usage performance
3.14 Qualification for Electro-migration	Demonstration using test structures that the metal layers will perform in the high current density condition	90 DUTs per metal layer. See JESD202	3	Accelerated test conditions of current density and temperature per JESD202	Sample failure; open or resistance change of +10%
3.15 Qualification of TFRs	to establish the reliability of TFRs; uses TFR test structure(s)	90 DUTs for TALT 5 for step stress	3	Follow 4-step process 1. ΔT Modeling 2. IR Temp. measurements 3. I or V step stress (5 DUTs) 4. TALT (90 DUTs) •Select 3 junction temperatures •Utilize TFR geometry with WC temp. rise; •current/voltage at max. per design rules; •at max die temperature	1% change in resistance
3.16 Qualification of Bulk Resistors	to establish the reliability of bulk resistors; uses bulk resistor test structure(s)	90 DUTs for TALT 5 for step stress	3	Follow 4 -step process 1. ΔT Modeling 2. IR Temp. measurements 3. I or V step stress (5 DUTs) 4. TALT (90 DUTs) • Select 3 junction temperatures •Utilize bulk resistor geometry with WC temp. rise •current/voltage at max. per design rules •at max die temperature	10% change in resistance
4.1 Air Sensitivity	To suggest that all qualifications be in alignment with the design choice of hermetic vs. nonhermetic for the applications	per specific qual sections	per specific qual sections	Hermetic - N_2 ; -or- Nonhermetic 30% to 70% RH	per specific qual sections
4.2 Moisture Sensitivity	For nonhermetic applications, demonstration that the device will perform after exposure to high RH	30 devices	3	•85 °C, 85% RH, 1,000 hours, •normal bias applied, readouts every 250 hours	Per Section 3.7

Test Description	Purpose	Sample Size	# of sample lots	Environment / Conditions	Failure Criteria
4.2.1 Ammonia RGA for Hermetic Package	To alleviate concerns about NH_3 reaction products from moisture with GaN die, AlN packages, etc.	6 hermetic packaged devices	3	•150 °C bake, 320 hours •Perform RGA test per MIL-STD-883K, Method 1018.10 •RGA Specific to NH_3	Presence of NH_3 (no limit is presently established)
4.3 Water Droplet Test	For nonhermetic applications, demonstration that the device will perform after exposure to condensed liquid water, which could turn to ice in space	6 devices	3	Room ambient, $V_{DSabs.max}$, Channel pinched off, 5-minute exposure	Any sample failures -or- Per Section 3.7
4.4 Hydrogen Sensitivity Test	Demonstrate that the device performance will not degrade when exposed to low level of trapped hydrogen from the packaging	12 devices	3	250 °C temperature, 1,000-hour exposure to forming gas; passive exposure	Per Section 3.7
4.5 Operation in Vacuum	Assure freedom from multipaction at device bondpads, bondwires, package	1 or per TOR-2014-02198	1 or per TOR	see TOR for detailed test and /or analysis procedures	See TOR for failure criteria based on either analysis or test
5.1 MIMCAP Qualification (destructive samples)	Using test structures, demonstrate that MIMCAP dielectric defect density is acceptable for the reliability needs of the product using the effective thickness model	500 DUTs, with total area 1000× product	3 min, then continuously	Apply voltage ramp of 5 V/sec until rupture at room temperature	•Compute reliability per Appendix F. •Criteria determined by mission
5.2 Gate Defects	Surrogate demonstration using test structures that the gate manufacturing defect density is acceptable for the reliability of the product	1,000× product	All, continuously	•Apply V_{DG} voltage ramp of 50 V/sec to at least $V_{DSmax.safe}$ with source open •Apply reverse V_{GS} voltage ramp of 50 V/sec to at least $V_{GSmax.safe}$ with drain open	•Shorts, or •gate-drain or gate source leakages failing specifications
5.3 Airbridge Defects	Demonstration that the manufacturing defect density for airbridge damage is acceptable for the reliability needs of the product	12 devices	3 lots	•Bake test at 300 °C for 1 hour •Product MMIC or HEMT •Test structure recommended	Any sample failures
5.4 Via Defects	Surrogate demonstration that the via process defect density is acceptable for the reliability of the product	100× the # of vias used in the product	3 lots	•Air-to-Air temperature shock (–55 °C to +250 °C, 50 °C/min), 50 cycles •Bake Test 250 °C for 1 hour; test structures or quantity of product die	30× inspection criteria for cracks, etc.; Change in resistance >10%
6.1 Backside Metal Adhesion	Demonstrate that the wafer backside metal adhesion is adequate for the reliability of the product	12 samples	at least 3 backside lots	Tape adhesion tests using ASTM D3330 as a guide	Any removed metal, any metal adhered to the tape

Test Description	Purpose	Sample Size	# of sample lots	Environment / Conditions	Failure Criteria
6.2 Bond Pull Test (destructive)	Demonstrate that the wirebonding process has adequate reliability	225 bonds total	3 wafers	Modified MIL-STD-883, Method 2011 • BOL bond group: - 25 bonds from each wafer; • EOL1 bond group - 25 bonds from each wafer after 300 °C, 360-hour exposure; • EOL 2 bond group - 25 bonds from each wafer after 300 °C, 72-hour exposure • Record destructive pull force • Compute lower conf. limits •Perform optical inspection at 15X on 3 bondpads w/ metal etched off	• per Fig. 2011-2 of MIL-STD-883K, Method 2011-10 using: •Au-Au preseal reqmts for BOL group •Au preseal rqmts for BOL group •Au post seal rqmts for EOL1 & EOL2 groups •No substrate damage or cracking (3 samples)
6.3 Die Shear	Demonstrate that the die attach process is adequate	6 die	3 bonding lots	MIL-STD-883, Method 2019	any sample failures
6.4 Step Coverage	Demonstrate that any metal stepdown in the device design meets the coverage requirements	samples per MIL-STD-883, Meth. 2018, Table I	samples from 2 wafers	MIL-STD-883, Method 2018	Method 2018 criteria, SEM inspections
6.5 Low-Frequency Oscillations	Demonstrate that no low-frequency oscillations are inherent in the device	3 devices	each sample from a unique lot	Gate pinchoff; V_{DS} = $V_{DSabs.max}$; ballast resistor connection; noise analyzer listening from 0.01 Hz to1 kHz	oscillations detected
7.3 Total Ionizing Dose (7.7.4 TID Test Plan)	Demonstrate total dose radiation hardness per environment of Section 7.7.2 or mission requirements	40	3	Co-60 source; bias at four Q-points (Figure 3-1); unbiased; two RF conditions; also controls	Per Section 3.7
7.4 Dose Rate – (7.7.6 Operate Thru Test Plan)	Demonstrate recovery after a radiation pulse per environment of Section 7.7.2 or mission requirement	14	3	Electron LINAC or FXR; Bias at point Q1(on) and Q4(off), also controls; V_{DS} > 120% of max. usage	recovery time requirement
7.4 Dose Rate – (7.7.5 Survival Test Plan)	Demonstrate immunity from burnout per environment of Section 7.7.2 or mission requirement	14	3	FXR; Bias at point Q1(on) and Q4(off), also controls; V_{DS} > 120% of max. usage	immediate burnout
7.5 Single-Event Effects–SEE (7.7.7 Proton Test Plan)	Demonstrate no failures from proton exposure per environment of Section 7.7.2 or mission requirement	27 max (fewer if DD per exposure is small)	3	Proton cyclotron; DC bias at point (Q4 off-state); RF bias under usage conditions; also controls	immediate burnout or upset
7.5 Single-Event Effects–SEE (7.7.8 Heavy Ions Test Plan)	Determine or bound the upset or burnout cross section characteristic vs. LET exposure per environment of Section 7.7.2 or mission requirement	39 (fewer if DD per exposure is small)	3	Cyclotron; DC bias at point (Q4 off-state); RF bias under usage conditions; also controls	immediate burnout or upset
7.6 Displacement Damage (DD) Effects (7.7.3 Neutron Test Plan)	Demonstrate immunity to neutron fluences exposure per environment of Section 7.7.2 or mission requirement	8	3	Nuclear reactor; passive irradiation followed by post-test; also controls	Per Section 3.7

Appendix B. Standards Referenced

This table lists external specifications and standards referenced in this guideline.

Document	Abbreviated Title	Description
MIL-STD-883K	Test Method Standards, Microcircuits	Collection of test methods for microcircuits, including monolithic, multichip, film and hybrid microcircuits, microcircuit arrays, and the elements therein
Method 1017.3	Neutron Radiation	Test methods for neutron displacement damage
Method 1018.10	Internal Gas Analysis	Test method for performing RGA for moisture and other gases in hermetic modules
Method 1019.9	Ionizing Radiation / Total Dose	Test method for total dose testing
Method 1020.1	Dose Rate Induced Latchup	Methods to determine latchup susceptibility in a pulsed dose rate environment
Method 1021.3	Dose Rate Upset of Digital Microcircuits	Methods to determine logic upset thresholds of digital circuits in a pulsed dose rate environment
Method 1023.3	Dose Rate Response & Threshold of Linear Microcircuits	Methods to determine the responses to and thresholds of linear/analog circuits in a pulsed dose rate environment
Method 2011.10	Bond Strength	Wire bond pull testing method and criteria
Method 2018.6	SEM Inspections	Rules and acceptance criteria for SEM inspection of die and microcircuit features, step coverage, metallization, etc.
Method 2019.10	Die Shear Strength	Die shear test method and criteria
Method 3015.9	Electrostatic Discharge Sensitivity Classification	Specifies classes of ESD sensitivity, provides the HBM test method
Method 5005.17	Qualification and Quality Conformance Procedures	Defines inspection and test procedures (Groups A–E) for microelectronics, defines quality class & radiation levels, QML certification
MIL-STD-750-1A w/Change 3	Environmental Test Methods for Semiconductor Devices	Collection of test standards for discrete semiconductors
Method 1017.1	Neutron Irradiation	Test method for neutron displacement damage
Method 1018.6	Internal Gas Analysis	Test method for performing RGA for moisture and other gases in hermetic modules
Method 1019.5	Steady-State Total Dose Irradiation	Test method for total dose testing
Method 1080.1	Single-Event Burnout & Gate Rupture	Method to test for destructive burnout in general devices and gate rupture in MOS devices from heavy ion exposures
MIL-HDBK-814	Ionizing Radiation & Neutron Hardness Assurance Guidelines	Statistical treatment of hardness data, RLAT rules
MIL-PRF-19500P	Performance Specification, Semiconductor Devices	Establishes the performance requisites of semiconductors, quality conformance directives. Has five quality levels, and 8 RHA levels, screening, lot acceptance rules, etc.
MIL-PRF-38534L	Performance Specification, Hybrid Microcircuits	Establishes the performance & verification requirements for hybrids and MCMs (multichip modules)
MIL-PRF-38535L	Performance Specification, Integrated Circuits (Microcircuits) Manufacturing	Establishes the requirements for manufacturing and test of ICs under multiple device quality classes, and RHA levels

Document	Abbreviated Title	Description
JEDEC JESD22-A.104D	Temperature Cycling	Provides temperature cycling method and determination of accelerated cycling life
JEDEC JESD22-C.101F	Field-Induced Charged Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components	ESD test requirements for the CDM
JEDEC JESD47-I.01	Stress-Driven Qualification of Integrated Circuits	Acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process that is being changed.
JEDEC JESD57A	Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation	Specifies test procedures and data interpretation for SEE
JEDEC JESD 91A	Developing Acceleration Models for Electronic Component Failure Mechanisms	Reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components
JEDEC JEP118A	Guidelines for GaAs MMIC PHEMT/MESFET and HBT Accelerated Life Testing	Establishes methods, quantities, and data analysis for GaAs multi-temperature lifetest
JEDEC JESD202	Electromigration Failure Time of Interconnects Under Constant & Temperature Stress	Defines test structures, methods, and analysis for EM testing
JEDEC JESD234	Proton Radiation Single-Event Effects in Semiconductor Devices	Establishes test procedures for performing proton exposures and interpreting results
JEDEC JESD15	Thermal Model Overview	Thermal modeling master document
JEDEC JESD51-1	IC Thermal Management Method	Determination of thermal characteristics of a single packaged IC die.
JEDEC JESD 51-14	Transient Dual Interface Test Method for the Measurement of Thermal Resistance	Test method for establishing thermal resistance from junction to case
JEDEC JEP110	Thermal Resistance in GaAs FETs	Established test procedure for measurement of GaAs device thermal resistance
ASTM D3359-09	Measurement of Adhesion	Contains tape pull test procedure
ASTM E1249-15	Minimizing Dosimetry Errors in Radiation Hardness Testing of Electronic Devices Using Co-60 Source	Procedures for measuring absorbed dose of a device in a Co-60 environment
ASTM F1892-12	Ionizing Radiation (Total Dose) Effects Testing	Establishes test sequences and data analysis procedures to characterize microelectronic devices for total dose
ASTM F1893-11	Ionizing Dose Rate Survivability & Burnout	Requirements for testing survivability and burnout of electronic devices in a high dose rate pulsed radiation environment
ASTM F1262M-14	Transient Radiation Upset Threshold Testing of Digital ICs	Guidelines for determining the transient radiation upset level of Si digital ICs in a pulsed radiation environment
ASTM F1263-11	Analysis of Overtest Data in Radiation Testing of Electronic Parts	Guide for determining the probabilistic survival threshold of electronic parts
ASTM E1854-13	Ensuring Test Consistency in Neutron-Induced Displacement Damage of Electronic Parts	Requirements for neutron-induced displacement damage testing in Si and GaAs devices
ASTM F980-16	Rapid Annealing of Neutron-Induced Displacement Damage in Si Semiconductor Devices	Requirements for testing Si discrete devices for annealing of displacement damage after a neutron pulse
ASTM E722-14	Characterizing Neutron Fluence Spectra in Terms of a Monoenergetic Neutron Fluence for Radiation Hardness Assurance Testing	Guideline for converting the neutron fluence from a source to an equivalent monoenergetic neutron fluence

Document	Abbreviated Title	Description
ASTM F1192-11	Single-Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices	Guide of performing tests needed to predict SEP rates in integrated circuits when exposed to space radiation
Aerospace TOR-2011(8591)-21	Mission Assurance Guidelines for A-D Mission Risk Classes	Establishes risk classes for programs and missions
Aerospace TOR-2006(8583)-5236 Rev. B	Electronic Parts, Materials, and Processes Used in Space and Launch Vehicles	Technical baseline in the selection, application, procurement, control, and standardization of parts; includes radiation requirements
Aerospace TOR-2014-02198	Standard/Handbook for Multipactor Breakdown Prevention in Spacecraft Components	Guidelines for multipaction testing, analysis and assessments
US DOD TRA2011	Technology Readiness Assessment (TRA) Guidance	Establishes levels for technology maturity and readiness for missions
ESA ESCC-22900	Total Dose Steady-State Irradiation	Procedures for assessing TID responses of electronic parts
ESA ESCC- 25100	Single-Event Effects Test Method	Testing and analysis methods for SEP of electronics
NASA Tech. Memo 4527	Natural Orbital Environment Guidelines for Use in Aerospace Vehicle Development	Defines the natural near-Earth space environment suitable for design of space vehicles

Appendix C. Acronyms

Less Common Acronyms	Extended Name
2DEG	two-dimensional electron gas
2TLT	two-temperature life test
3TLT	three-temperature life test
AFR	average failure rate
AFRL	Air Force Research Laboratory
ALD	atomic layer deposition
ASTM	American Society for Testing and Materials
BOL	beginning of operational life
CDI	cumulative damage index
CDM	charged device model
CW	continuous wave
DC	direct current
DD	displacement damage
DIVA	dynamic current (I) vs. voltage (V) analyzer
DLOS	deep-level optical spectroscopy
DLTS	deep-level transient spectroscopy
DOD	Department of Defense
DOE	design of experiments
DUT	device under test
DWV	dielectric withstanding voltage
ELDRS	enhanced low dose rate sensitivity
EMMI	emission microscopy
EOL	end of operational life
ESA	European Space Agency
ESD	electrostatic discharge
FA	failure analysis
FIB	focused ion beam
FIT	failures in time (alternatively, “failure unit”)
FOD	foreign object debris
FWHM	full width, half maximum

Less Common Acronyms	Extended Name
FXR	flash xray
GEE	gate end-to-end (resistance)
HBM	human body model
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
HTOL	high temperature operating life
HTRB	high temperature reverse bias
IC	integrated circuit
I-DLTS	current mode deep level transient spectroscopy
IDSS	drain current at zero gate voltage
IEL	ionizing energy loss
IG	insulated gate
IGA	internal gas analysis
IR	infrared
IV	current (I) vs. voltage (V)
IVT	current (I) vs. voltage (V) v. temperature (T)
IPE	inverse piezoelectric effect
JAXA	Japan Aerospace Exploration Agency
JEDEC	Joint Electron Device Engineering Council
LD-MOSFET	laterally diffused metal-oxide-semiconductor field effect transistor
LED	light emitting diode
LET	linear energy transfer
LFO	low-frequency oscillation
LINAC	linear accelerator
LNA	low-noise amplifier
MEO	medium Earth orbit
MIL STD	military standard
MIMCAP	metal insulator metal capacitor
MIS	metal insulator semiconductor
MLCC	multilayer ceramic capacitor
MM	machine model
MMIC	monolithic microwave integrated circuit

Less Common Acronyms	Extended Name
MOCVD	drain current at zero gate voltage
MOSFET	metal-oxide-silicon field effect transistor
MOS	metal oxide silicon
MTF	median time to failure
MTTF	mean time to failure
MWIR	medium wavelength infrared
N_2	nitrogen gas (N_2)
NIEL	nonionizing energy loss
NSS	national security space
PAE	power added efficiency
PCM	process control monitor
PECVD	plasma enhanced chemical vapor deposition
PEM	plastic encapsulated microcircuit
PIV	pulsed current (I) vs. voltage (V)
PMPCB	Parts, Materials, and Processes Control Board
QML	qualified manufacturers listing
Q-point	quiescent point
RF	radio frequency
RGA	residual gas analysis
RH	relative humidity
RLAT	radiation lot acceptance testing
RPP	rectangular parallelpiped
s11, s21, s12, s22	two-port scattering parameters as defined in microwave network theory
SCFP	source-connected field plate
SEB	single-event burnout
SEC	standard evaluation circuit
SEDR	single-event dielectric rupture
SEE	single-event effects
SEFI	single-event functional interrupt
SEGR	single-event gate rupture
SEL	single-event latchup
SEP	single-event phenomena

Less Common Acronyms	Extended Name
SET	single-event transient
SEU	single-event upset
SEM	scanning electron microscope
SERS	surface enhanced Raman spectroscopy
SOA	safe operating area
SP	signature parameter
SPA	semiconductor parameter analyzer
SPC	statistical process control
SRH	Shockley-Read-Hall
TALT	temperature-accelerated lifetest
TBD	to be determined
TBR	thermal barrier resistance
TCR	thermal coefficient of resistance
TDDB	time-dependent dielectric breakdown
TEM	transmission electron microscope
TFR	thin film resistor
THB	temperature humidity bias
TID	total ionizing dose
TLYF	test like you fly
TRA	technology readiness assessment
TRB	technology review board
TRL	technology readiness level
TSP	temperature sensitive parameter
TSST	temperature step-stress test
VALT	voltage-accelerated lifetest
VDS	drain to source voltage
VNA	vector network analyzer
VSST	voltage step-stress test
VSWR	voltage standing wave ratio
WCCA	worst-case circuit analysis

Appendix D. Origin and Discussion of GaN HEMT Ratings

This appendix is a more detailed discussion of electrical ratings appropriate for GaN HEMTs and MMICs. The GaN technology is sufficiently different from Si or GaAs to require an adjustment in the approach taken to ratings and deratings. The following comments attempt to address this issue. A recommended derating approach for GaN HEMTs is provided.

D.1 Drain Voltage Ratings

Unlike their GaAs HEMT or Si power MOSFET (metal-oxide-semiconductor field effect transistor) brethren, GaN HEMTs do not have a sustainable well-defined breakdown or avalanche voltage. In GaN HEMTs, an avalanche breakdown that is caused by a cascade of ionized carriers through a region of semiconductor with a high imposed electric field does not readily occur. (There are no pn junctions in HEMTs and no body diodes). Since GaN is highly piezoelectric, the application of high electric fields in GaN HEMTs develops a mechanical strain. This strain can cause traps and broken bonds to form, forming a conducting path, and leading to rapid breakdown. There appears to be a critical electric field above which traps begin to be formed. The degree to which the applied electric field exceeds this critical field is key. For fields only slightly higher than the critical field, traps are formed slowly and manifest as leakage current and gradual performance degradation. For excess fields significantly higher than the critical field, breakdown is more rapid, becoming nearly instantaneous and catastrophic when the excess field is sufficiently high. It is important to characterize this critical field (or critical voltage V_{crit}) for high-reliability space missions. Where the RF loadline exceeds V_{crit}, reliability assessments are needed.

The consequences of a transient overvoltage condition in many wide bandgap materials and devices can be much more serious than the same event in silicon or GaAs devices. The failure signature is more like that of a ceramic capacitor overvoltage event that shows a sudden catastrophic failure. An important component of a high-reliability space program is the WCCA (worst-case circuit analysis). A WCCA endeavors among other things to show that all ratings and deratings of components are met. It is important for device manufacturers and users to understand the nature of GaN HEMT voltage ratings and deratings. Figure D-1 shows a comparison of breakdown voltage in a Si LD-MOSFET, a ceramic capacitor, and a GaN HEMT. This figure illustrates simplistically the nature of breakdown in the different devices as current versus voltage.

Figure D-1a shows the drain-source breakdown rating $V_{(BR)DSS}$ for a typical LD-MOSFET (laterally diffused metal oxide semiconductor field effect transistor). LD-MOS devices are widely employed as RF power amplifiers and are slowly being displaced by GaN HEMTs, which are quickly becoming more affordable. The drain-source breakdown voltage is a well-defined parameter where avalanche current rises predictably above the voltage $V_{(BR)DSS}$. The manufacturer provides a recommended Q-point (quiescent point) at 26 V for Class A or Class AB amplifiers and a rated breakdown voltage $V_{(BR)DSS}$ of 65 V. Derating guidance is provided in Aerospace document TOR-2006(8583)-5236 rev. B (Robertson, 2006) such that the maximum voltage shall not exceed 80% of breakdown, or 52 V. Further derating may be required to survive single-event effects, such as single-event burnout.

On the other hand, a multilayer ceramic capacitor (MLCC) does not have a well-defined breakdown voltage. Consider a typical ceramic capacitor with a nameplate maximum voltage rating of 63 V in Figure D-1b. The guiding document requires a voltage derating at 85 °C of 80% of maximum for nominal operation and 50% for worst case. Nominal operation is defined as normal steady-state mission conditions, whereas worst-case operation describes atypical transients, power-up conditions, etc. (see Robertson, 2006 for details). At 125 °C, the voltage derating is more conservative, becoming 50% for nominal and 30% for worst case. These large safety factors exist because of the time-dependent nature of

the sudden catastrophic failures that occur in ceramic capacitors. High-reliability MLCCs are generally required on a lot sampling basis to survive a 1,000-hour HTOL (high-temperature operating life) test at 2× the rated voltage, as shown in Figure D-1b. Elevating the voltage to higher and higher values causes catastrophic failures at shorter and shorter times as shown.

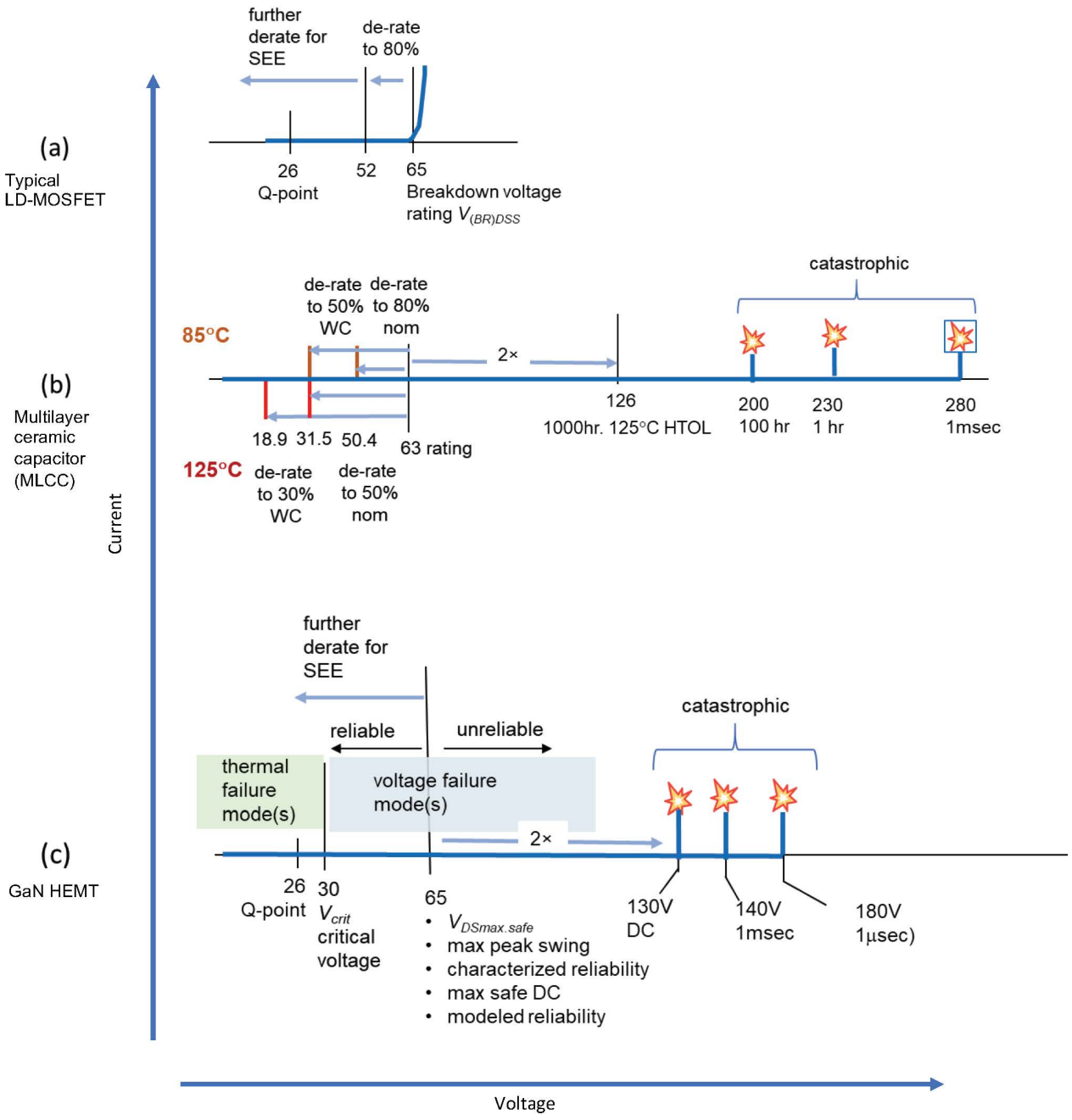


Figure D-1. Simplified representation of the breakdown characteristics of (a) a typical LD-MOSFET, (b) a multilayer ceramic capacitor, and (c) a GaN HEMT. The GaN HEMT in many ways resembles the capacitor more than the Si LD-MOSFET since it exhibits catastrophic breakdown rather than a sustaining breakdown voltage.

A GaN HEMT behaves more like a ceramic capacitor than a typical Si semiconductor device. Figure D-1c shows that there is also a catastrophic breakdown effect—the value becoming higher and higher for shorter and shorter durations. In Section 2.1 of this document, the method of determining the SOA (safe operating area) is discussed. It is recommended here to set the safe value of drain voltage $V_{DSmax.safe}$ to be such that the lower 3σ value of measured catastrophic breakdown events lies at least 2× to 3× higher than $V_{DSmax.safe}$. It is further discussed in Sections 3.1 and 3.2 that because there are voltage-driven failure modes possible when operating above V_{crit}, the value of $V_{DSmax.safe}$ may be further constrained to a yet lower value. Finally, as discussed in Section 7, single-event effects (especially single-event burnout, SEB) may further constrain the value of the $V_{DSmax.safe}$. Reliability is generally controlled by thermally driven failure modes below V_{crit}. However, because of the possibility of SEB, $V_{DSmax.safe}$ may need to be specified to a value even below V_{crit}. Testing for SEB decides this issue for a space environment.

It is believed that leakage current is the trigger for the catastrophic breakdown observed at sufficiently high voltages in a GaN HEMT. The catastrophic breakdown is in some ways like that in a typical dielectric material. In a dielectric, once the current flow is initiated, a conducting channel or path is formed that is permanent. In ESD (electrostatic discharge) tests of GaN HEMTs, the initiation of the conduction channel via a snapback effect happens on the time scale of nanoseconds (Tazzoli, 2007). In other cases, the presence of a small leakage current path can cause similar effects. Some of the leakage paths under off-state operation that can trigger such an event are shown in Figure D-2 by the numbered green arrows as follows:

- Thermionic field emission of electrons (from gate metal to the AlGaN barrier on the drain side)
- Leakage current along the AlGaN surface, the Si_3N_4 passivation, or the interface between the two
- Leakage current between the drain electrode and the substrate, especially if a substrate barrier does not exist, or if the substrate is Si

Note that the arrows show electron currents rather than conventional currents. Under on-state conditions (or more colloquially, in the “semi-on” state), an additional mechanism may be present:

- Hot-carrier generation on the drain side of the gate

Hot carriers are generated in the “cloud” region shown in Figure D-2. Hot electrons are generated when the instantaneous operating point moves to the right side (high-voltage) side of the IV plane. The hot carriers can create new traps, damage the interface, and degrade the 2DEG. All are reliability concerns. Figure D-2 shows a conventional HEMT structure without a field plate. Field plates are effective in spreading out and lowering the electric fields in the susceptible region between the gate and drain. Devices with field plates may achieve a higher catastrophic breakdown voltage.

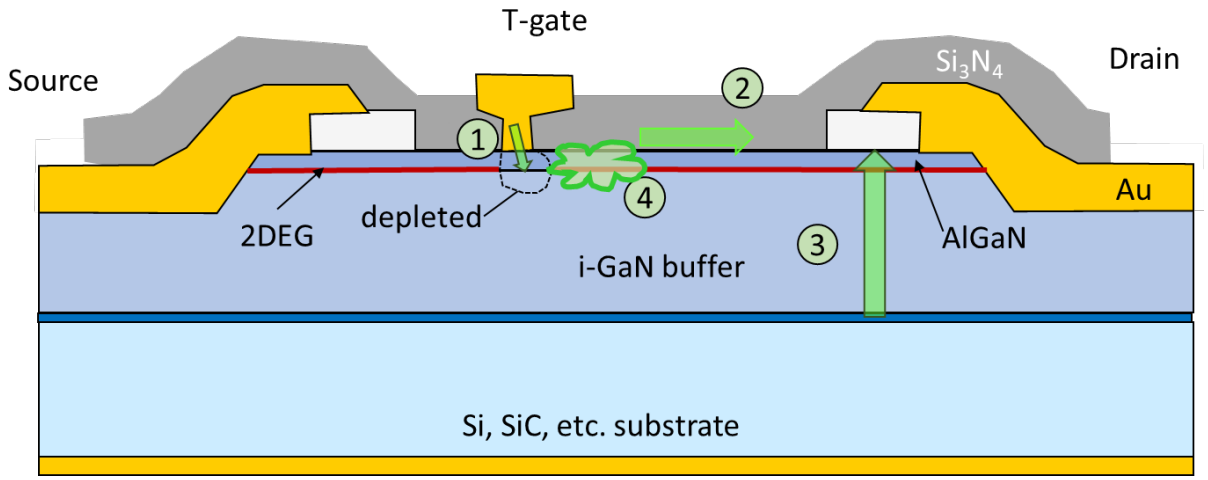


Figure D-2. Simplified GaN HEMT cross section showing the current leakages that could possibly trigger catastrophic breakdown: (1) thermionic field emission, (2) surface leakages, (3) drain-substrate leakage, and (4) hot carrier generation. The arrows denote electron currents rather than conventional currents.

It is quite possible (and becoming generally accepted at this time) that these noncatastrophic leakages can also cause time-dependent breakdown. In other words, if a high-voltage or high-field condition exists that is not immediately catastrophic, continued operation under this condition will eventually lead to a premature catastrophic breakdown. This type of phenomenon is reminiscent of TDDB (time-dependent dielectric breakdown) that is the classic mode of breakdown in MOS gate insulators, MIMCAPs, and other dielectric structures. It has been found that this type of time-dependent breakdown occurs in GaN HEMTs above a certain critical voltage V_{crit}. It is classified as a voltage-driven intrinsic failure mechanism. Often, V_{crit} is well below the instantaneous catastrophic breakdown voltage. In Section 3.4, a recommended method of determination of V_{crit} using a voltage step-stress is described.

For all these reasons, the maximum drain voltage rating for a GaN HEMT has a much different meaning than for other conventional devices. Since there is no sustaining avalanche ionization mechanism, specifying a percentage derating factor against a breakdown voltage is not a meaningful concept for GaN HEMTs. Unfortunately, there has been no real standard or guidance regarding voltage ratings amongst the GaN manufacturers until this time. To correct this situation, the following recommendation is made here.

D.1.1 $V_{DSmax.safe}$ Rating Recommendation

It is recommended that manufacturers provide a maximum safe drain voltage rating $V_{DSmax.safe}$ according to the following:

- Such that –3σ limit of off-state burnout voltages (see Sections 2.1 and 2.2) when measured under DC (1 sec duration) conditions is at least 2× to 3× higher than $V_{DSmax.safe}$
- As determined by a stated assured reliability (see Section 3.2 and Appendix H), for example, 0.2% failures with 90% confidence after a 15-year mission at maximum temperature. The reliability requirement may be tailored.
- With safety margin against SEB (Sections 7.7.7 and 7.7.8) as needed

The minimum of these three constraints shall be taken as the value of $V_{DSmax.safe}$. This rating may be translated to a rating for the drain-gate maximum safe voltage by subtracting $V_{GSmax.safe}$, the maximum safe

gate reverse voltage rating (see below). In that case, the off-state drain SOA measurements should be conducted at the rated $V_{GSmax.safe}$.

Many of the GaN HEMT applications are microwave power amplifiers. For these, it is recommended that during usage at the highest compression level under worst-case conditions, the peak voltage traversed in the RF cycle not exceed this maximum safe value. Figure D-3 shows the relationship between the catastrophic breakdown voltage, the critical voltage V_{crit}, the quiescent voltage V_Q the maximum safe voltage rating $V_{DSmax,safe}$, and the peak operating voltage V_{pk} of the transistor. This figure shows the common source characteristic curves of a HEMT and the SOA (safe operating area). The catstrophic breakdown voltage is far away from the maximum safe rated drain-source voltage.

Other complications arise for GaN HEMTs used in RF amplifiers. Typically, the device is biased at a certain quiescent point (Q-point) at which the voltage and current are maintained with zero RF signal. Then when the RF drive is applied, the voltage swings about this Q-point. Consider the two loadlines in Figure D-3—one is a simple Class A loadline and the other a more complex harmonically tuned class F^{-1} loadline. The more complex loadline may have loops or reentrant segments, depending upon the circuit design. At high frequencies, the loadlines widen into load "figures" due to the reactances associated with the load and the device itself. The Q-points (shown by the dots in Figure D-3) for each amplifier class may be located at differing places in the IV plane. The peak voltage V_{pk} for both of these loadlines is located at the lower right corner of the IV plane, where the current is minimum (or zero). The value of V_{pk} may be 2–3× higher than the quiescent voltage, depending upon the specifics of the amplifier RF design. It is important that the value of V_{pk} not exceed the $V_{DSmax.safe}$ rating. Thus, the quiescent voltage is 2–3× less than the peak voltage V_{pk}, which in turn is 2–3× less than the catastrophic breakdown voltage.

The value of V_{crit} is controlled by the fabrication process and transistor construction. The value of V_Q is a circuit design choice of the amplifier class. The value of V_{pk} is a circuit design attribute of the power supply voltage and the loadline. The rating $V_{DSmax.safe}$ is reliability driven. The catastrophic breakdown voltage BV (and its -3σ lower statistical bound) is related to the transistor design and materials. Of all of these voltage properties, V_{crit} is the most variable. V_{crit} could be lower than V_Q or higher than V_{pk}. It may not exist at all if the HEMT does not show a voltage dependence of time-to-failure. See Section 3.2 for details on incorporation of V_{crit} into reliability models, and Section 3.4 for its measurement.

A series of off-state ramped breakdown tests should be performed to establish the catastrophic breakdown locus as described in Section 2.2. The appropriate limit (the -3σ value is recommended) of the statistical distribution of these catastrophic breakdown voltages should be at least 2–3× higher than the drain voltage rating $V_{DSmax.safe}$. More conservatism may be needed for the reliability assurance and for the possibility of SEB.

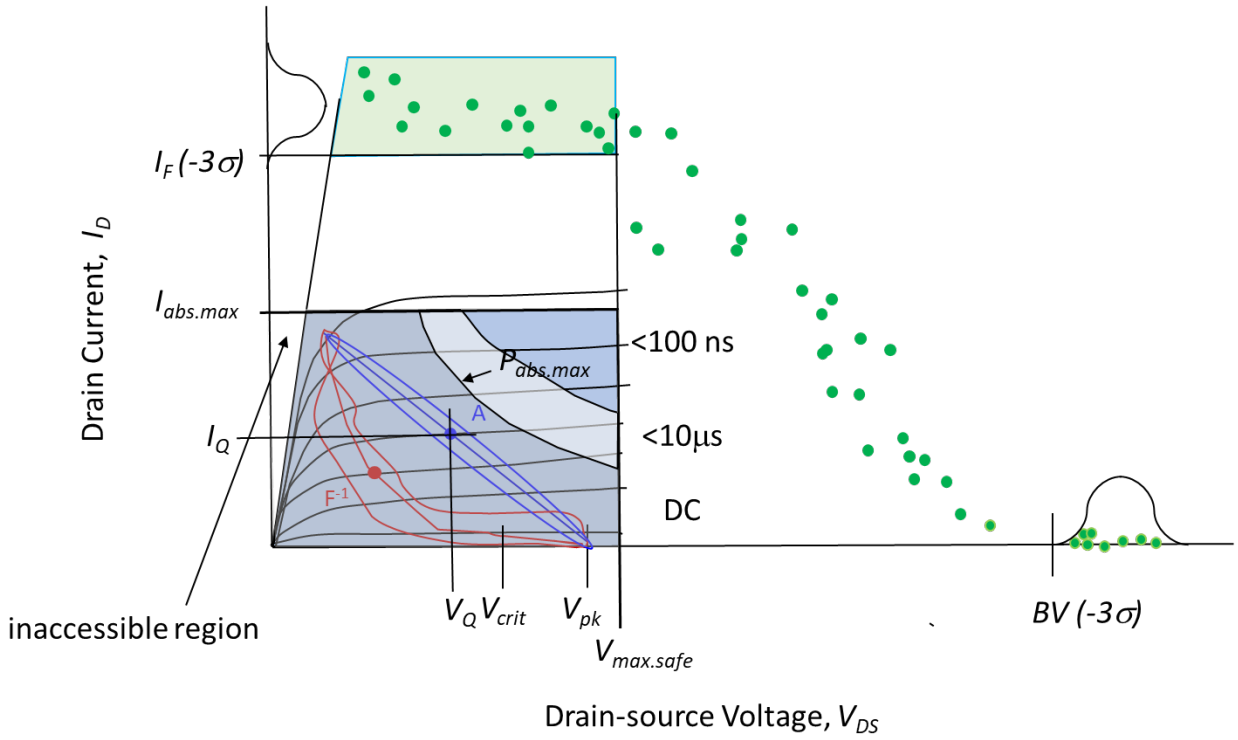


Figure D-3. Common source IV curves for a typical GaN HEMT, showing the relationship between rated maximum safe drain-source voltage $V_{DSmax.safe}$ as recommended here, the catastrophic breakdown BV (and its -3σ limit), the peak operating voltage V_{pk}, and the critical voltage V_{crit}. Two typical load figures and their quiescent bias points are shown for a Class A and Class F^{-1} amplifiers. Also shown is the rated maximum safe drain current $I_{Dmax.safe}$ as recommended here. Its relationship to the failure current I_F (and its -3σ limit) is shown by the green-shaded region. The DC SOA and pulsed SOA regions at various pulsewidths are shown by the shaded regions. The dots show typical DC burnout/ parameter degradation points.

D.2 Drain Current Ratings

Determination of the SOA as described in Sections 2.1 and 2.2 covers burnout points at various drain currents. The locus of burnout points as shown in Figure D-3, if not immediately catastrophic, is felt as a sudden degradation in parameters such as R_{Don} leakage currents, transconductance, etc. It is important that the maximum safe drain current rating at the top of the SOA be located conservatively away from this locus of points. For this data to be valid, the thermal environment of the test transistors must be similar to that of transistors in usage. It is recommended that the maximum safe drain current rating $I_{Dmax.safe}$ be placed such that the -3σ value of all the failure currents I_F measured with the drain voltage less than $V_{DSmax.safe}$ are at least 2× the value of $I_{Dmax.safe}$. In other words, the ratio of I_F (-3σ) to $I_{Dmax.safe}$ is no less than 2. See Figure D-3 for an elucidation of the locations of these high current points by the green quadrilateral figure. Note that there is an inaccessible region of the SOA that is limited by the resistance of the HEMT, R_{Don}. Approximate constant power hyperbolae define the regions that are limited by a maximum power dissipation. For shorter pulsewidths, the SOA may be extended by the additional shaded regions as shown. For a sufficiently short pulsewidth, the SOA becomes squared off at the corner ($I_{Dmax.safe}$, $V_{DSmax.safe}$) where power dissipation is highest. The mapping of the SOA power hyperbolae may be accomplished with aid of thermal simulations.

D.2.1 $I_{Dmax.safe}$ Rating Recommendation

It is recommended that users provide a maximum safe drain current rating $I_{Dmax.safe}$ according to the following:

- Such that –3σ limit of all on-state burnout current points (see Section 2.1) that lie below $V_{DSmax.safe}$ when measured under DC (1 sec duration) conditions is at least 2× higher than $I_{Dmax.safe}$. See Figure D-3 for clarification.

D.3 Gate Voltage/Current Ratings

Still more complications occur when the amplifier is driven into compression or is overdriven. Under conditions where the input power P_{in} is high, additional stressing of the HEMT occurs, necessitating further consideration of deratings. Figure D-4 shows a typical P_{out} vs. P_{in} characteristic of a HEMT amplifier driven beyond the linear region into compression. The average DC gate current is also shown in this plot. The average DC gate current is initially negative (conventional current flowing *out* of the gate terminal) at low input power. At low P_{in}, the negative quiescent gate bias voltage is only slightly modulated by the relatively small RF signal. Under linear uncompressed operation, this gate current is negative and relatively small, being composed mostly of the Schottky diode reverse current. Figure D-5 shows waveforms at the intrinsic gate terminal. As P_{in} is raised, the RF voltage swing becomes larger and larger, eventually beginning to forward-bias the gate Schottky diode (red curve in Figure D-5). As the amplifier begins to enter compression, the DC average gate current rises rapidly as the RF signal is rectified by the gate Schottky diode. Under heavily compressed operation, the high forward bias gate current during the forward RF cycle is accompanied also by a high reverse gate voltage during the reverse cycle, as shown by the blue curve in Figure D-5. Thus, the high positive average DC gate current is also an indicator of a high reverse gate voltage during each half-cycle. Note that it is not always possible to observe these gate waveforms in an actual HEMT amplifier circuit, especially at high frequencies. The problem is that the parasitic capacitances and inductances prevent access to the "intrinsic" transistor. In a sense, the peak positive gate current and peak negative gate voltage may not be observable. Therefore, it is recommended that appropriate maximum safe values be placed on measurable DC quantities.

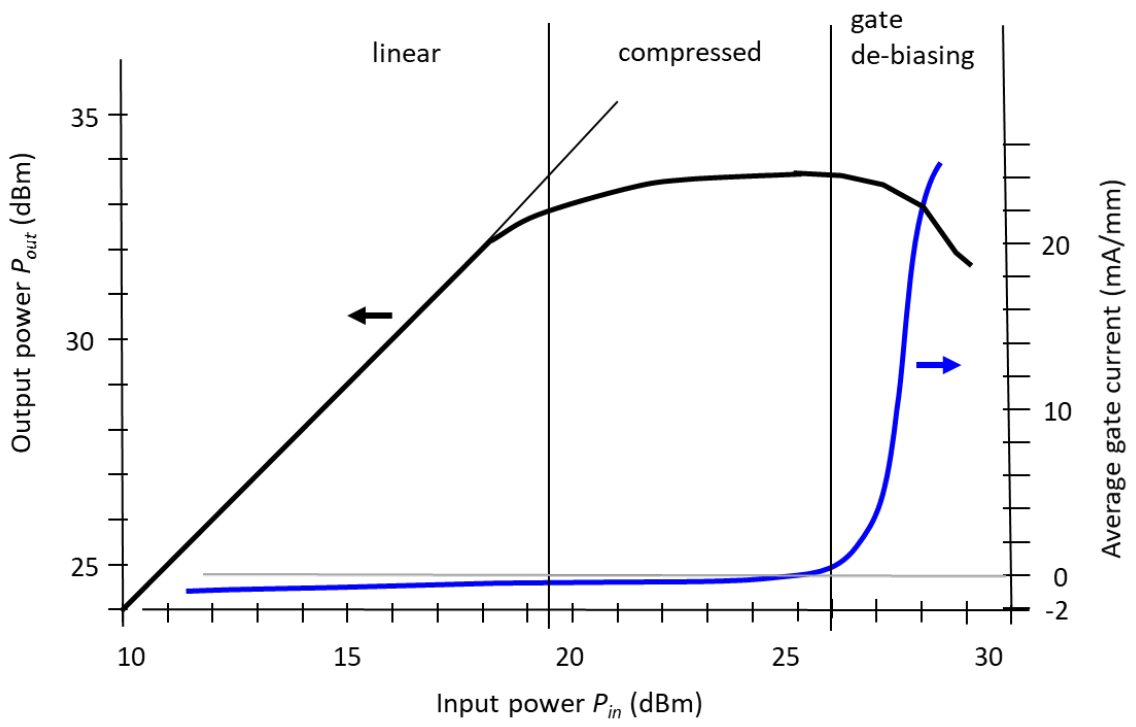


Figure D-4. A typical output power vs. input power sweep of a GaN HEMT or MMIC. The accompanying average DC gate current is an indicator of the degree of compression.

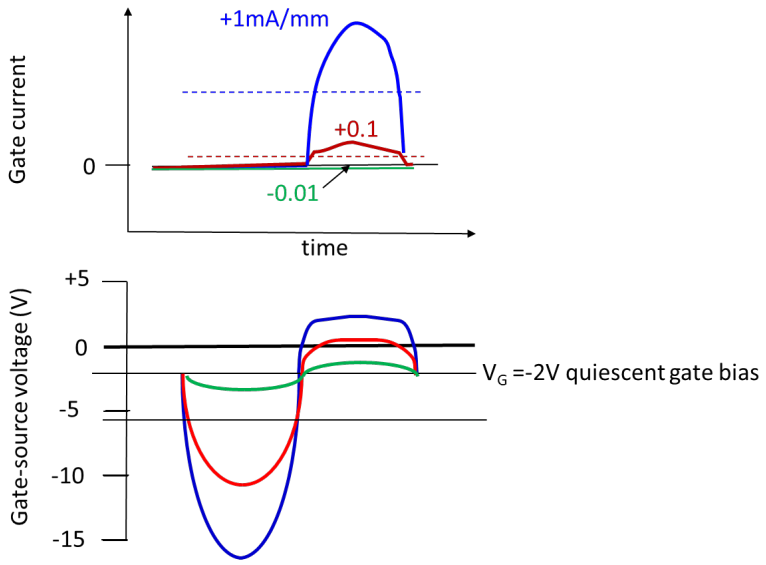


Figure D-5. Gate voltage and gate current waveforms at the "intrinsic" transistor for various RF drive levels that generate –0.01 (uncompressed), +0.1 (compressed), and +1 mA/mm (heavily compressed) of DC average gate current. Corresponding gate voltage waveforms are shown. There is no debiasing of the gate in these waveforms.

Furthermore, under high RF drive, the gate may become "debiased." This happens when the rectified RF forward current competes with intentionally supplied DC bias current. (See Section 3.10.1 for more details on gate debiasing). The HEMT DC bias voltage may become less negative or change polarity when under RF drive.

If a HEMT is overdriven and the gate is debiased only slightly or not at all, failure may occur by either an excessively high forward peak gate current or by an excessively high reverse peak gate voltage. Which failure mode occurs first depends upon the device and circuit design. High forward gate bias may lead eventually to failure because of electromigration in the gate finger or by the thermal damage to the Schottky barrier. High reverse gate voltage can lead to catastrophic gate breakdown by the identical failure modes identified in Figure D-1. Under reverse gate bias, the device is fully pinched off, and an electric field exists in the region between the gate and source regions. The catastrophic gate-source breakdown voltage is smaller than the gate-drain breakdown voltage because the gate-source spacing is smaller than the gate-drain spacing. Leakage current mechanisms 1 and 2 (Figure D-2) are able to trigger a reverse V_{GS} catastrophic breakdown at a lower voltage than between the drain and gate. Therefore, the SOA for rated maximum safe reverse gate voltage must by geometrical necessity be much lower than the maximum safe rated drain-source voltage.

For highly compressed or overdriven HEMTs, it is recommended that an absolute maximum limit be placed on the DC average forward gate current. This limit is best defined by the gate SOA test procedures as described in Section 2.3, since there appears to be little or no correlation between gate current under RF drive and reliability at this time. This is very different from GaAs HEMTs where the gate current can clearly signal hot electron generation and damage under overdrive. For GaAs HEMTs, a conservative criterion of 0.1 mA/mm of absolute gate current is typically exercised. No such criterion can be recommended for GaN HEMTs. A similar argument can be made for the peak maximum safe reverse gate voltage $V_{GSmax.safe}$. It is best taken from the measured gate SOA as described in Section 2.3. It should be defined as the value such that the –3σ value of reverse gate breakdown events are at least 2× to 3× higher than the value of $V_{GSmax.safe}$. The peak reverse excursion of gate voltage should not exceed this value in compression.

D.3.1 $V_{GSmax.safe}$ Rating Recommendation

It is recommended that a maximum safe reverse gate voltage rating $V_{GSmax.safe}$ be provided according to the following:

- Such that $+3\sigma$ limit of reverse gate voltage burnout points (see Section 2.3 and Figure D-3) when measured under DC (1 sec duration) conditions is at least 2× to 3× lower (more negative) than $V_{GSmax.safe}$. Note that since gate burnout voltages are negative, the $+3\sigma$ limit is needed for this comparison.

D.3.2 $I_{Gmax.safe}$ Rating Recommendation

It is recommended that a maximum safe forward gate current rating $I_{Gmax.safe}$ be provided according to the following:

- Such that the –3σ limit of all forward gate SOA burnout current points (see Section 2.3 and Figure D-3) when measured under DC (1 sec duration) conditions at least 2× higher than $I_{Gmax.safe}$.

D.4 Ratings Standard for GaN HEMTs and MMICs

Based upon the discussions in this appendix, a proposed standardized approach for GaN HEMT ratings for high-reliability space missions is shown in Table D-1. A similar standardized ratings table for a GaN MMIC fabrication process is shown in Table D-2. In these tables the following definitions have been made:

- A "reliability goal" expresses that in a certain number of years the probability of failure does not exceed a certain value with a certain confidence. (Note: Specifying a median time to fail MTF would be equivalent if the statistical distribution were also stated, i.e., a lognormal distribution or Weibull with a certain shape factor. However, this is not generally done.)

- The temperature T_{max} refers to the maximum channel temperature commensurate with the above reliability goal.

- Maximum safe drain voltage $V_{DSmax.safe}$ refers to a maximum safe RF peak instantaneous drain voltage or DC voltage rating. Some conditions must be met:

    - The catastrophic drain breakdown voltage shall be 2–3× higher than $V_{DSmax.safe}$.
    - Operation at a continuously applied DC voltage less than or equal to $V_{DSmax.safe}$ and at a temperature below T_{max} ensures that the reliability goal above is met.

- Note that $V_{DSmax.safe}$ may be further constrained by single-event burnout (SEB). See Section 7. The critical drain voltage V_{crit} refers to the drain voltage above which drain and gate leakage currents become time dependent. Above V_{crit} the leakages gradually increase in time and performance degrades in time with a rate dependent on the drain voltage. At the maximum safe drain voltage $V_{DSmax.safe}$, the reliability goal above is still met.

- The maximum safe drain current $I_{Dmax.safex}$ refers to the maximum safe peak instantaneous drain current under RF or DC conditions. The drain current at which failures or degradations occur is at least 2× higher.

- Absolute maximum reverse gate-source voltage $V_{GSmax.safe}$ refers to a maximum safe RF peak instantaneous gate voltage or DC gate voltage rating. The catastrophic gate-source breakdown voltage shall be 2–3× higher.

- A recommended drain quiescent DC voltage Q-point may optionally also be specified; however, the circuit designer should be responsible for ensuring that $V_{DSmax.safe}$ and $V_{GSmax.safe}$ are never exceeded.

- An SOA (safe operating area) refers to the regions in the I_{DS} vs. V_{DS} plane or the I_{GS} vs. V_{GS} plane for which the reliability goal is fully met under DC operation. The SOA is a combination of thermal, voltage, and current limits. The SOA may be extended for pulsed operation based upon temperature rise allowable.

- The RF survivability refers to a particular set of recommended standard conditions (pulse repetition frequency, pulsewidth, duration, etc.) and may be tailored as needed for specific missions or requirements.

In Table D-1 is a recommended example maximum ratings table that might be constructed for a space-grade, high-reliability GaN HEMT. This is a fictitious device for example purposes only. By obeying these ratings, full performance could be expected per the stated reliability goal. Note the absence of a breakdown voltage rating, since this is not a meaningful concept as stated above. Instead, the maximum safe voltage rating as described above is utilized. Both pulsed DC and pulsed RF burnout levels are provided as supplementary ratings. Both have pulsewidths of 1 msec. The maximum channel temperature is provided along with a maximum thermal resistance, so that any translations to pulsed or DC power can be made based upon the baseplate temperature. The baseplate temperature may be interpreted as the die back surface (for die products) or the back surface of the case (for packaged products). The maximum

temperature rating always trumps the current and/or voltage ratings. All the current ratings are shown here for illustration purposes in units of current density (mA/mm); however, for a particular transistor, these units could be converted to absolute currents (mA or A), unless elsewhere the gate width is provided. The recommended Q-point illustrates common class AB operation within band. It is implied that by operating in this manner, even up to 3 dB compression, the other ratings—particularly the gate current rating—would still be met, as long as T_{max} is not violated.

Many other details are missing from this absolute maximum ratings Table D-1, such as maximum soldering temperatures, storage temperature, humidity, maximum screw torque (for flange packages), etc. These are beyond the scope of this appendix.

In Table D-2 is a similar example maximum ratings table for a MMIC process. Since a process specification does not always have a specific device size in mind, the thermal resistance parameter presents a difficulty. Therefore a device with a standard geometry is called out, and the thermal resistivity (°C-mm/W) rather than thermal resistance (°C/W) as for a specific device. The geometry specified here may be tailored in accordance with conventions of the MMIC fabrication facility.

It is highly recommended that these maximum ratings for high-reliability, space-qualified GaN HEMTs and MMIC processes be standardized according to this approach.

Table D-1. Example Maximum Ratings Table for a Space-Grade, High-Reliability GaN HEMT (Note the intentional absence of a "breakdown voltage" BV rating, since this is not necessarily a useful concept for GaN HEMTs.)

Maximum Ratings[1]	Symbol	Rating	units	
Maximum channel temperature	T_{max}	250	°C	T_{max}
Maximum Safe Drain-Source Voltage[2]	$V_{DSmax.safe}$	70	V	T_{max}
Maximum Safe Drain Current per unit gate width	$I_{Dmax.safe}$	850	mA/mm	T_{max}
Maximum Safe Reverse Gate-Source Voltage	$V_{GRmax.safe}$	-12	V	$V_{DS} = V_{DSmax,safe}$, T_{max}
Maximum Safe Gate Current per finger[3]	$I_{Gmax.safe}$	2	mA	electromigration limit
Maximum Safe RF Input Power[4]	$P_{in.max.safe}$	28	dBm	CW, input return loss < 15dB, f = band center, T_{max}
Maximum Safe RF Dissipated Power	$P_{diss.max.safe}$	33	W	CW

[1]Operation within these maximum ratings meets the reliability goal of 0.2% failures in 15 years with 90% confidence
[2]DC or pulsing above $V_{DSmax.safe}$ reduces reliability and risks immediate or delayed catastrophic breakdown
[3]DC or average RF gate current
[4]for full recovery of performance within 1 sec after exposure

Supplementary Rating	Symbol	Rating	units	
Channel-to-Baseplate Thermal Resistance	θ_{CB}	1.5	°C/W	specified at T_{max}
Critical Voltage[5]	V_{crit}	25	V	specified at T_{max}
Recommended Quiescent Voltage[6]	V_Q	35	V	
Recommended Quiescent Current[6]	I_Q	180	mA/mm	
Burnout Drain-Gate Voltage[7]	$V_{DG(BO)}$	140	V	1 msec DC pulse, T = 25°C
Burnout RF Input Power [7]	$P_{in(BO)}$	32	dBm	PW=10μsec, PRF=1kHz, f = band center, for 1 min., T = 25°C

[5]Operation above V_{crit} incurs performance degradations still within EOL limits if max safe ratings are obeyed.
[6]For typical class AB operation with compression less than 3dB
[7]Catastrophic burnout ensues within 1 minute of application of this applied condition

Table D-2. Example Maximum Ratings Table for a Space-Grade, High-Reliability GaN HEMT MMIC Process. Some of the units and conditions are adjusted as compared to Table D-1 as appropriate for a MMIC.

Maximum Ratings[1]	Symbol	Rating	units	conditions
Maximum channel temperature	T_{max}	250	°C	T_{max}
Maximum Safe Drain-Source Voltage[2]	$V_{DSmax.safe}$	70	V	T_{max}
Maximum Safe Drain Current	$I_{Dmax.safe}$	850	mA/mm	T_{max}
Maximum Safe Reverse Gate-Source Voltage	$V_{GRmax.safe}$	-12	V	$V_{DS} = V_{DSmax,safe}$, T_{max}
Maximum Safe Gate Current per finger[3]	$I_{Gmax.safe}$	2	mA	electromigration limit
Maximum Safe RF Input Power per unit gate width[4]	$P_{in.max.safe}$	0.12	W/mm	CW, input return loss < 15dB, f = band center, T_{max}
Maximum Safe RF Dissipated Power per unit gate width	$P_{diss.max.safe}$	6.6	W/mm	CW, f = band center, T_{max}

[1]Operation within these maximum ratings meets the reliability goal of 0.2% failures in 15 years with 90% confidence
[2]DC or pulsing above $V_{DSmax.safe}$ reduces reliability and risks immediate or delayed catastrophic breakdown
[3]DC or average RF gate current
[4]for full recovery of performance within 1 sec after exposure

Supplementary Rating	Symbol	Rating	units	conditions
Channel-to-Baseplate Thermal Resistivity	θ'_{CB}	16	°C-mm/W	T_{max}, *4 x 400um device*[5]
Critical Voltage[6]	V_{crit}	25	V	T_{max}
Recommended Quiescent Voltage[7]	V_Q	35	V	
Recommended Quiescent Current[7]	I_Q	180	mA/mm	
Burnout Drain-Gate Voltage[8]	$V_{DG(BO)}$	140	V	1 msec DC pulse, T = 25°C
Burnout RF Input Power per unit gate width[8]	$P_{in(BO)}$	1.5	W/mm	PW=10μsec, PRF=1kHz, f = band center, for 1 min., T = 25°C

[5]Specified for a standard geometry with 4 fingers each 400um wide. Larger geometries have higher thermal resistivity.
[6]Operation above V_{crit} incurs performance degradations still within EOL limits if max safe ratings are obeyed.
[7]For typical class AB operation with compression less than 3dB
[8]Catastrophic burnout ensues within 1 minute of application of this applied condition

Appendix E. Temperature Measurements

This appendix is based upon material graciously provided by Eric R. Heller, Air Force Research Laboratory, Dayton, OH.

The prediction of wearout failure in GaN HEMTs or MMICs requires that data be taken from accelerated tests. Among the stress factors that accelerate failure, temperature is one of the key drivers, along with electric field, stress gradient, and possibly others. But arguably, temperature may be the most important driver. In accelerated testing (and in the mission or application), knowledge of the temperature is required to determine acceleration factors. Typically, failures are driven by kinetics that have an Arrhenius relationship in temperature. The "activation energy" derives from an analysis of the temperatures at which accelerated testing is performed and is used to extrapolate to usage temperatures to determine reliability. Methodologies are described in JEDEC Standard (JEP118A and by Scarpulla (2000).

But GaN is different from other materials (e.g., Si, GaAs). The primary difference is in the magnitude of its thermal effects (temperature rise, temperature transients, gradients, etc.). Previously overlooked factors, such as the thermal barrier resistance between GaN and substrate, the extremely high temperature gradients, etc., may lead to errors. Existing JEDEC standards such as JESD 15, JESD 51-1, JESD 51-14, and JEP 110 should be followed when they are applicable but may be inadequate. This appendix attempts to address some of the deficiencies by covering four issues:

- General recommendations
- Specific caveats for temperature determination in GaN HEMTs
- A brief survey of thermography techniques
- Benefits and tradeoffs of thermal modeling

E.1 General Recommendations

It is important to minimize temperature errors as much as possible and to obtain temperatures that are meaningful given the failure mode. The failure mode can occur in various regions of the GaN HEMT or its surroundings. In the HEMT itself, the failure region might be directly under the gate, in the access region, at an ohmic contact, etc. (see Figure 1-1 for the many possibilities). The recommended DC accelerated testing at the four Q-points in Figure 3-1 is intended to stress different physical regions of HEMT devices. In a MMIC, the failure might be in one of the conductors, in a TFR, or a MIMCAP. Each of these failure regions, whether located in the HEMT itself or in an ancillary region of the MMIC, will be characterized by a unique failure mechanism and failure kinetics with a distinct activation energy. The one mechanism with the shortest failure time when translated to mission usage conditions should be the one of most interest.

Therefore, it is important to have knowledge of the temperature in the region of interest. In many cases, the region of interest is inaccessible, or at best difficult to access. For example, the region under an airbridge or in the depletion zone directly under a gate are obscured. In these cases, modeling comes to the aid in the determination of the local temperature in a particular region of interest. For example, if the temperature of a non-airbridged region can be measured, translating to the region of interest can be accomplished using finite element thermal modeling. Similarly, if the temperature of the gate electrode itself can be measured, a translation to the depletion zone under the gate may be possible. When this sort of translation is performed using modeling, an inference is made about the temperature in the region of interest. It is important to quantify any temperature errors that might creep in because of making this inference, and to incorporate these errors into the final time-to-failure estimates and projections.

Even if it is possible to directly measure temperature in a particular region of interest, inferences are still usually needed. For one, temperature measurements at accelerated conditions must be translated to temperature values under mission usage conditions. For another, it may not be possible to make temperature measurements at the exact accelerated test condition—a combination of a baseplate temperature (hot/cold plate temperature, oven temperature, etc.) and the temperature rise associated with dissipated power. Temperatures therefore are usually translated from available temperature measurement conditions to accelerated test conditions and are further translated to mission usage conditions. Any errors incurred by these translations are reflected in errors in the final projected failure times and reliability metrics. It is important to quantify these errors and include them in reliability predictions.

E.2 Specific Caveats in the Measurement of Temperature

The following offers some more specific areas requiring special attention in the temperature assessments of GaN devices. These areas may require extra validations, tighter measurement tolerances, more uncertainty quantification or higher-fidelity models than needed in previous GaAs or Si technologies.

- **Large Temperature Gradients.** Where testing requires significant power dissipation, temperature gradients will also be significantly large. The temperature will vary rapidly by location. Roughly, the temperature gradient scales with the power density, inversely with the size of the power dissipation region (for example, the depletion zone) and inversely with the thermal conductivity of the materials through which the heat must pass as it reaches the baseplate or heatsink (Heller, 2013). An analogy can be made between GaN and GaAs HEMT devices: GaN can support roughly 10× the power density as GaAs (in units of W/mm), with a roughly similar size of the heat-dissipating region (the depletion zone) (Yamamura, 2011). The thermal conductivity of GaN is only modestly better than GaAs. Therefore, the thermal gradients are many times higher for the GaN case, as is the concomitant temperature error arising from sampling area or volume considerations.

- **Large Temperature Differences from Channel to Baseplate.** The absolute temperature difference between the failing region of interest and the baseplate, case, or heatsink temperature is much higher in GaN devices than for GaAs or Si by dint of the higher power dissipation. A given percentage error in thermal resistance will translate to a larger absolute error in the temperature. In addition, the temperature dependence of the thermal resistance must be considered. If neglected, this will cause a temperature error roughly proportional to the square of the power dissipation. Errors in the neglect or inaccuracy of the thermal resistance of this sort are especially egregious. Accuracy in temperature estimations requires that the thermal resistance be expressed as a function of the power, baseplate temperature, and bias condition.

- **Fast Transients.** When pulsed-power conditions are required in RF-driven lifetesting or TLYF testing, there will be transients. Effective thermal time constants scale with the thermal diffusivity and inversely with the size of the heat-dissipating region. In some cases, most of the heating is observed in the first microsecond of the power pulse (Manoi, 2011; Maize, 2013). For pulsewidths on this time scale or less, estimation of the temperature rise may be a difficult proposition. Relating the pulsed power lifetimes to lifetimes obtained in DC testing could be challenging. For this reason, there are benefits to performing TLYF tests in these circumstances.

- **Deviations from Ideal Cooling.** The thermal conductivities and thermal diffusivities vary greatly as heat travels from the GaN to the substrate thence to the baseplate or heatsink. This is doubly true for the thermal boundary resistance between GaN and the substrate. This drives a large deviation in the ideal cooling characteristic. In JEDEC standard JESD51-14 (2010), a peak

temperature estimation is based upon the assumption that a "temperature sensitive parameter" (TSP) varies as the square root of time upon removal of a power pulse. (A TSP is an electrical property such as a metallization resistivity, Schottky barrier voltage, etc., that is amenable to a transient temperature coefficient measurement.) The assumption behind this method is that the effective thermal resistance remains fixed so that a straight-line cooling curve can be plotted of the TSP vs $t^{1/2}$. This assumption may not be true for the GaN materials since thermal resistance may vary significantly during the cooling pulse. Further, some materials such as SiC have a large temperature dependence to thermal conductivity, and some, such as alloyed metals, may have a much more modest temperature dependence. Where both kinds of materials are large contributors to the overall thermal resistance and over wide temperature ranges, the nature of the cooling curve may vary with temperature enough to require consideration.

- **Thermal Boundary Resistance (TBR) and Complex Thermal Paths.** The TBR, the GaN, and the substrate all have different thermal properties. This means that the thermal path from the heat dissipation region to the baseplate is complex. When the TBR is relatively high in older epi processes, for example (Kuball, 2010), it greatly complicates the thermal path. Therefore, the effective thermal resistance may be unexpectedly high.

- **High Arrhenius Activation Energies.** For GaN HEMTs, many of the failure mechanisms have relatively high activation energies approaching 2 eV. This is higher than the typical activation energies of about 1 eV for legacy Si or GaAs technologies. A higher activation energy incurs a higher temperature sensitivity in accelerated tests and magnifies the effect of temperature errors on the predicted reliability. On the other hand, usage at a higher temperature (closer to the accelerated testing temperature) counters this error sensitivity somewhat. Note also that a very high activation energy increases the likelihood that a "hidden" or "sneak" mode might exist that has a lower activation energy. In this event, high-temperature accelerated testing may detect the higher activation energy mode, while lower temperature usage may fail under the lower activation energy mode (see Section 3.1.2).

E.3 A Brief GaN-centric Survey of Thermography Techniques

There are many ways in current practice to measure the same thing—temperature at the failure site. However, measurement techniques vary greatly in exactly where the temperature is measured, and under exactly what conditions the reported temperature is accurate. This section is intended to guide the user to a best estimate using techniques that may be available.

- **IR (Infrared) Passive Thermography**

  - **Principle of Operation.** In this technique, the infrared light intensity over a range of wavelengths emitted by the hot surface of the DUT is used to determine the temperature (MacDonald, 1997). This requires a microscope with MWIR (medium wavelength infrared) optics, a heated stage, and possibly micro-manipulators for probing the DUT. An IR camera or focal plane array is used to capture an image. The system is calibrated with little or no power applied to the DUT while it is heated passively to one or more temperatures by the heated stage. Thus, the intensity-to–surface temperature relationship is defined. Then when under operating power dissipation, this relationship is used to establish the surface temperature. The sample may be coated with graphite in order to make it more emissive. The data collected is in the form of a 2D map.

- **Lateral Resolution.** The lateral spatial resolution is diffraction limited, usually to about 2–10 μm, depending on the wavelengths detected. So, it is not capable of resolving temperature variation across a gate length of 0.25 μm, for example. If the drain-source spacing in a HEMT is 3 μm, this may (at best) barely exceed the diffraction limit. This limits the usefulness of IR thermography for determination of the region of power dissipation in the channel or recess as a function of bias. However, the technique is useful for determining the higher-scale temperature distribution, for example, across a 100 μm finger width, or the difference in temperature between a central finger as compared to an end finger. It is a good sanity check on other thermography methods and can reveal hot spots. If the DUT has been coated, the lateral spatial resolution worsens by the addition of approximately twice the coating thickness. This can be substantial, since a typical graphite coating might be as much as 1–2 mils in thickness (up to ~25–50 μm).

- **Vertical Resolution.** The vertical resolution is good, being essentially the top surface, as long as the material surface is opaque with emissivity >0.2. However, GaN and SiC are transparent to IR wavelengths. Then the temperature measured is that of the first opaque material encountered from the top. This could well be the back surface of the die, which is an undesirable situation.

- **Temporal Resolution.** The time necessary to collect an IR image can be seconds to minutes, depending upon the temperature differential and the infrared emissivity.

- **Sample Preparation.** The DUT must be a probe-able die or de-lidded packaged device that can be placed on the temperature stage or hot/cold plate. In some cases, a coating with graphite material aids in improving the image.

- **Error Sources.** The main source of error with IR thermography is related to the temperature differential above ambient. If the differential above ambient is too small, there will not be enough IR signal above background for accurate measurements. Another source of error is if there are reflective or mirrorlike surfaces such as Au. GaN and SiC are largely transparent at MWIR wavelengths, and this can be a large source of error as measured emission “from the channel” will in that case come largely from optically opaque layers under the substrate. Graphite may contribute to alternate current paths due to its electrical conductivity, which can alter MMIC operation or contribute to parallel heat loads. Besides their low emissivity, these surfaces will tend to reflect IR from various sources in the room and create errors. Background IR, especially if the DUT is near room temperature, may contribute to error, although many systems will perform a calibration to measure and subtract this background.

- **Availability.** Commercial IR microscope systems are available and can be operated successfully by trained technicians.

- **Thermoreflectance**

  - **Principle of Operation.** A fast, pulsed light source—usually a laser or LED—is synchronized to a pulsed bias, for example, a pulsed electrical load or a pulsed drain voltage (Matei, 2017). The percentage change in the reflectance of the light at a certain selected interface, for example, a passivant/air interface, varies with temperature. This “thermoreflectance coefficient” is the signal of interest. This is often parts to tens of parts per million per degree and may require averaging many frames to quantify. Typically, “hot”

and “cold” reflectance are measured rapidly back and forth to resolve the slight reflectance difference, making this technique best suited for thermal transients. Typically, the wavelength of the light source is chosen to maximize this thermoreflectance coefficient and is usually sub-bandgap. A calibration in which the ambient temperature is ramped with the device dissipating little or no power is used to obtain the thermoreflectance coefficient. What is needed is an optical microscope, microscope camera sensitive to very slight changes in intensity, software algorithm to do the appropriate averaging, hot/cold stage, and possibly micromanipulator probes. The data is usually in the form of a 2D map. The focused light spot can be scanned over the DUT or the entire image frame may be illuminated.

- **Lateral Resolution.** The lateral resolution is the diffraction limit of the imaging camera, typically less than 1 μm. The ability to discern temperature variations across a channel region or access region in a HEMT is likely to be very good, although this is still under investigation.

- **Vertical Resolution.** The thermoreflectance technique measures the surface of the DUT at the air/passivation interface or the air/metallization interface. If there are multiple thin and transparent layers, the vertical resolution becomes compromised by multiple reflections.

- **Temporal Resolution.** The measurement times can be subnanosecond, limited by the laser pulse duration. A sampling technique can be used to average over many pulses to obtain a good signal-to-noise ratio.

- **Sample Preparation.** The DUT must be a probe-able die or a de-lidded packaged device that can be placed on the temperature stage or hot/cold plate. The DUT is pulsed with electronic equipment that must be compatible with the instrument for synchronization purposes. As with any pulsed power configuration, electrical transients must be well controlled.

- **Error Sources.** This is a somewhat immature technique, and the nature of the errors is still under investigation. Issues exist with vastly different thermoreflectance coefficients for different materials, providing ambiguous temperature readouts. Also, rough or mottled surfaces cause difficulties.

- **Availability.** This is a newer technique, with at least one vendor selling a commercial system. An applied research lab may be required to obtain useful results for samples with complex topography, different interfaces, and μm-scale features. A skilled technician may be capable of handling simpler DUTs.

- **Micro-Raman Scattering (Bulk)**

  - **Principle of Operation.** When an incident photon from a monochromatic light source (such as a laser) interacts with a molecule, there is a small chance (approximately 1 photon in 10^6) that it will be scattered inelastically. Inelastic scattering means that the photon interacts with the collective motion of the molecular bonds of GaN, SiC, or other crystalline materials, producing a change in vibrational energy. This is usually a loss of energy “Stokes shift” accompanied by creation of a phonon, but can be a gain “anti-Stokes shift” when a phonon is consumed instead. A better way to state this is that the photons inelastically scatter from optical phonons. The Raman technique measures a characteristic change in wavelength exhibited by the scattered photon. At different temperatures, the GaN bond

lengths change slightly, as do the phonon mode energies, and the Raman shift shows an empirical temperature dependence. The temperature dependence of this characteristic wavelength shift has been calibrated for GaN phonon modes (Liu, 1999) and is the basis of a thermography technique. Improved methods may use multiple Raman lines, measure the line width as well as the wavelength shift, or even measure the ratio of Stokes to anti-Stokes scattered photons (or a combination of these methods) to more accurately measure temperature. A grating spectrophotometer is used with a CCD detector to generate an optical spectrum displaying the characteristic Raman peaks. If the DUT is ramped in temperature with little or no dissipated power, the calibration of temperature can be found. Then when operating and dissipating power the wavelength shift of the scattered light is an indication of the temperature of the illuminated region.

- **Lateral Resolution.** The spot size is diffraction limited by the wavelength of the laser probe and also dependent on the optical path and numerical aperture of the focusing lens. It is typically about 1 μm. This allows the variation in temperature in the recess region along the width of a HEMT to be mapped. The dependence of the thermal profile on the bias condition can be investigated using Raman scattering. The difference in temperatures of the inner versus outer fingers in a multifinger HEMT can be displayed with Raman scattering (Kuball, 2003).

- **Vertical Resolution.** An average temperature of the entire thickness of GaN located in a cylindrical column under the laser spot is obtained. High numerical aperture confocal optical systems can give some depth sensitivity. With care, the temperature of the GaN and the temperature of the underlying substrate can be separately assessed because the Raman peaks are separate.

- **Temporal Resolution.** With a fast pulsed laser, the time resolution can be very fast, with subnanosecond resolution possible. Many sources use a CW laser for steady-state measurements.

- **Sample Preparation.** The DUT must be a probe-able die or a de-lidded packaged device. Only visible GaN regions can be measured, with no field plates, airbridges, or obscuring metal layers. Very tall or high aspect ratio structures can pose difficulties because the typical Raman setup employs high numerical aperture lenses for small spot size.

- **Error Sources.** Not only are the scattered photons sensitive to the temperature, but they are also sensitive to mechanical stress/strain (a tensor for GaN). If care is not taken, this will interfere with the temperature measurement. More accurate approaches utilize multiple Raman peaks scattered from different optical phonon modes to separate the stress from the temperature (Liu, 1999), consider linewidth and/or Stokes to anti-Stokes ratio. The Raman technique can have good accuracy but has a low signal-to-noise ratio requiring long integration times. Careful setups are required. An above-bandgap laser wavelength has been proposed to make the Raman measurements sensitive only to the surface of the GaN. However, this will excite local electron–hole pairs, altering the electrical conduction of the HEMT, and thus distorting the temperature reading. If a conventional sub-bandgap visible laser is used it still may alter trapping states in the GaN or AlGaN, producing a local threshold voltage shift under the laser spot. Then the electrical current in that region is changed by some percentage, also distorting the temperature readout.

- **Availability.** Raman or micro-Raman spectrometers are available from scientific instrument makers; however, a full system suitable for measuring GaN HEMTs with prober, hot stage,

optics, and microscope must be assembled from scratch. This is a laboratory technique requiring technical experts.

- **Surface-Enhanced Raman Spectroscopy (SERS) with Nanoparticles**
  - **Principle of Operation.** Nanoparticles can be purchased with known Raman responses (Kniepp, 2006) as a function of temperature. These may be seeded everywhere on the surface of a GaN HEMT or selectively on a region or structure of interest. For example, nanoparticles can be placed on a gate, atop a field plate, or in the drain-gate recess. If the particles are sparser than the laser spot size, individual ones can be queried, giving nanometer resolution.
  - **Lateral Resolution.** Depending upon the density of the nanoparticles, the lateral resolution can be excellent, as long as the location of the particles is well defined. It is possible to greatly improve upon the diffraction limit of the laser light.
  - **Vertical Resolution.** The nanoparticles are deposited on the surface, and the bulk GaN is no longer involved. Therefore, the vertical resolution is essentially the size of the nanoparticles. This is much better than bulk micro-Raman spectroscopy.
  - **Temporal Resolution.** The temporal resolution is similar to bulk micro-Raman spectroscopy, the laser pulse characteristics being the deciding factor. The signal-to-noise ratio will differ, however.
  - **Sample Preparation.** A special coating is needed, containing the nanoparticles. Access to regions of interest not covered by airbridges or field plates is needed for this method. A coat-able, probe-able die is needed, and a probe station is required; alternatively, a de-lidded packaged device is needed.
  - **Error Sources.** The technique is still maturing. Error sources have not been fully quantified.
  - **Availability.** This is a new and promising laboratory technique requiring expert practitioners, a repeatable nanoparticle coating process, and well-characterized Raman spectra. No commercial equipment is available at this time; however, the technique is rapidly being developed (Kniepp, 2006).

- **Gate Resistance Thermography**
  - **Principle of Operation.** If a special HEMT test structure is fabricated with gate feeds at both ends of the device, a resistance measurement can be made of the gate line. Sometimes this is referred to as a "gate end-to-end" (GEE) measurement (Paine, 2016). The gate line behaves like a metal film resistor typically 10–100 Ω in resistance, with a calibratable temperature coefficient. By passing a small current end to end, the temperature is obtained from the resistance value. The temperature-to-resistance relationship is determined while the HEMT test structure is dissipating little or no power. This relationship is then used as a calibration factor to determine the average temperature along the whole width of the gate. The method allows the temperature to be obtained in gates obscured from optical access, such as under an airbridge or field plate. It may also be used under RF conditions with precautions.

- **Lateral Resolution.** The lateral temperature resolution is essentially that of the gate length itself averaged over the entire width.

- **Vertical Resolution.** For common RF designs with submicron gate height and length, an excellent conductor of heat such as Au, is essentially isothermal vertically through the thickness. The vertical resolution is that of the height of the gate finger.

- **Temporal Resolution.** With careful implementation, the response can be fast, but dependent upon the electronics and setup.

- **Sources of Error.** For fast measurements, electrical transients can cause errors. Fast transient currents that charge or discharge the gate capacitance are error sources. The gate leakage must be small compared to the current used to measure the gate end-to-end resistance. The measurement current must be large enough to observe a signal with sufficient resolution, but not so large as to cause a large voltage drop along the gate line. If this voltage drop is large compared to ($V_{GS} - V_{th}$), then one end of the channel will be biased on more heavily than the other and lead to erroneous results. Careful test structure design is required to overcome these issues. With sufficiently high temperatures, the multiple metals in the gate metal stack can intermix or anneal. The temperature coefficient of the gate end-to-end resistance can then change and must be recalibrated. Finally, the external path of the current (aside from the intended gate end-to-end resistance) must have a low resistance so as not to interfere with the measurement. To eliminate this issue, a four-wire configuration can be used, at the expense of greater test structure complexity. Under RF drive, the HEMT test structure may not behave exactly like an actual HEMT.

- **Availability.** A special test structure must be fabricated to perform this measurement. It may be probed or packaged. The test structure need not have optical access. A hot chuck or hot/cold plate is required to calibrate the resistance vs. temperature relationship.

- **Liquid Crystal Thermography**

  - **Principle of Operation.** A coating consisting of nematic liquid crystals in a carrier solution is applied to the surface of the DUT and allowed to dry. The liquid crystal solution exhibits a phase change (from crystallinity to an undifferentiated liquid) at a certain temperature (Burgess, 1999). Solutions with various phase change temperatures, referred to as "clearing points," are available. A polarizing light source is used with a microscope to reveal the transition from liquid crystal to liquid. A hot/cold chuck is not necessary; however, it is desirable to vary the temperature about the transition point while the DUT dissipates a constant power.

  - **Lateral Resolution.** The lateral resolution is claimed to be a few microns but depends upon the thickness of the coating. The clearing point region will move as the power dissipation is increased so determining the highest temperature point can be somewhat subjective.

  - **Vertical Resolution.** The technique measures the surface temperature.

  - **Temporal Resolution.** This is essentially a steady-state temperature measurement. The time necessary to create the phase change is many seconds. The DUT can be varied in temperature through the transition temperature in a steady-state power dissipation mode.

- **Sources of Error.** It is claimed that under ideal circumstances, the liquid crystal transition temperature is known to within 0.1 °C. However, the technique relies on the ability to apply the coating in a consistent manner, with a controlled thickness. The liquid crystal coating can measure temperatures accurately only at its transition temperature, so in order to view temperature rises at different places, the power dissipated in the device must be changed, or the hot/cold stage temperature must be varied. This limitation can produce errors.

- **Availability.** This is an older technique, and only a few sources of liquid crystal material are available. It is inexpensive and sufficiently accurate to estimate the thermal resistance in many cases. For larger structures, such as TFRs or bulk resistors, it is a useful method. A technician practiced in the art of applying the coating and observing and interpreting the transition is needed.

- **Schottky Diode Thermography**

  - **Principle of Operation.** Since the Schottky barrier height and the forward voltage are exponentially temperature dependent, with proper calibration the diode voltage can be used as a temperature monitor (Darwish, 2008). Ordinarily, GaN HEMTs require a negative gate bias for proper operation. The method works by pulsing to forward bias to observe the resulting gate current, while controlling the drain current with a current limiter or pulsing it off temporarily. The forward gate current under constant gate voltage, (or alternatively, the forward gate voltage at constant gate current) is the "temperature-sensitive parameter," TSP. By operating at different dissipated powers, the temperature rise and thermal resistance can be ascertained. A calibration of the TSP must be performed first at various temperatures with the DUT dissipating little or no power.

  - **Lateral Resolution.** This technique provides an average temperature of the metal-semiconductor surface along the entire width of the gate. Its resolution is that of the gate length itself averaged over the entire width.

  - **Vertical Resolution.** The Schottky diode metal-semiconductor interface measures the temperature. The vertical resolution is essentially the dimension of that interface, a few nanometers.

  - **Temporal Resolution.** With the correct setup, it can be less than a microsecond. The method requires the drain voltage to be removed (or drain current limited) prior to the application of the forward gate bias. That time delay limits the temporal resolution.

  - **Sources of Error.** Trapping in the gate surface can change the forward characteristic of the diode, and if there are many pre-existing traps, the transients associated with the switching to forward bias may distort the temperature measurement. The time delays in establishing and measuring the forward voltage or current also contribute to errors in the temperature. The method provides an averaged temperature spatially over the gate width, not the peak temperature in the center of the width dimension, as might be desired. It also averages over all the fingers, unless a special one-finger device or test structure is fabricated. Even then, this is not the same thermal environment as an actual multifinger device and may produce different temperature estimates. Because the Schottky diode turn-on is exponential in nature, the "average" will not be a simple arithmetic average but instead will be weighted. This weighting will become more nonlinear as power (and temperature gradient along the gate width) increases.

- **Availability.** This method can be performed using any standard HEMT with a gate Schottky and need not be probed. A hot/cold plate is needed for the temperature calibration along with pulsed test equipment to supply the forward pulses and extract the voltage/current waveforms. A skilled electronics technician can perform the measurements.

E.4 Benefits and Tradeoffs of Thermal Modeling

Each of the temperature measurement techniques presented above has its limitations. The failure region of interest in a HEMT may not be exactly the location most amenable to an accurate measurement of temperature. Many of the techniques provide a spatially averaged temperature over an extended region, such as along the width of a gate finger or in a roughly cylindrical volume illuminated by a laser spot. In many cases the failing region of interest is obscured. In other cases, the power dissipation during the measurement may need to be different than the usage dissipated power. In other cases, the ambient or baseplate temperature must be unlike the actual usage temperature. For all these reasons, thermal modeling and simulation can be beneficial. If the thermal model in a given region or averaged over a certain region predicts a temperature in agreement with that measured in the same region, then success is achieved. If it does so across a range of power levels, then success is doubly achieved. If not, then either the measurements or the model is incorrect, and more work is needed. Achieving this correlation between model and measurement is the goal. Inferences then may be drawn that bridge from the simulated/measured region or power level to the failure region and power level of interest. Obtaining the most accurate estimate of the temperature in the failure region at the test or usage condition is necessary to make reliability predictions.

Two slightly different thermal modeling/simulation approaches are available—one simpler than the other. The simpler approach is a direct thermal simulation. Here a heat source volume (a region of thermal generation) is assumed a priori. For example, this might be a thin region approximating the 2DEG near the pinchoff point at the drain edge of the gate. Similarly, a heat sink or baseplate temperature is assumed to exist for example the back surface of the die attached to an isothermal plane, or a heat sink further removed from the device package. The space in between is the thermal path, and all layers, interfaces, and volumes are modeled. Finite element or finite difference software can used to solve the heat flow equation in two or three dimensions. In some cases, an analytical solution of a specific geometry can be obtained with some simplifying assumptions (Muzychka, 2013). For a simulation to be effective, all the thermal properties and dimensions of the materials in the thermal path must be known. Material properties of interest are the thermal diffusivity, thermal conductivity, specific heat, etc. Material properties are commonly a function of the temperature, leading to nonlinearities in the temperature rise vs. power, for example. Details such as the thermal barrier resistance (TBR) and its temperature coefficient between GaN and SiC, the thermal effect of voids in solder die attach, the removal of heat from ribbon bonds, etc., must be considered. Once the thermal simulation is set up and validated against measurements, it becomes an extremely useful tool for simulating the temperatures of interest in both accelerated testing and in usage applications. It can be used for both steady-state or transient temperature predictions.

Another more complicated thermal modeling approach is called electrothermal modeling. Here, rather than specifying the heat source directly, the electrical quantities such as terminal voltages or current densities are supplied as inputs. The simulator uses a finite elements analysis or finite differences analysis to model the semiconductors, insulators, and metals that make up the device. An analytical electrothermal solution is rarely attempted. Electrothermal simulation begins with the theory describing semiconductor device physics, including the Poisson equation, the drift-diffusion equation(s), hydrodynamic equations, and/or the energy balance method. They are used to obtain internal currents and electric fields within a HEMT or another device. The heat generation sources are developed (e.g., for drift-diffusion transport) as the vector dot product of the current density vector and the electric field vector in each subdomain, or

finite element. The temperature dependencies of all the material quantities such as electrical conductivity, carrier density, Fermi-level, etc., are included in an electrothermal simulation. In this fashion a coupled thermal and electrical simulation is provided. The result is a more accurate representation of the behavior of the device but comes at the cost of much more complexity. More expertise and more sophisticated software are needed to perform electrothermal simulations as compared to direct thermal simulations. Rather than simulating an entire device and its packaging, it is sometimes convenient to perform full electrothermal modeling of the 2DEG and channel in two dimensions (usually in cross section along the gate length and height dimensions) and connect this to a three-dimensional direct thermal simulation of the package and heat sink. This can save computation burden.

To quantify the errors that are associated with either the direct thermal or the electrothermal modeling approaches, several steps are recommended. When using finite difference or finite elements methods to solve the problem, the simulation volume will be filled with many subdomains or elements. The tradeoff is that more and smaller elements are needed for a more accurate but slower simulation vs. fewer coarser ones. It is always a good idea to optimize the size and number of domains or elements. Some regions (e.g., heat sink) will tolerate elements orders of magnitude larger than others (e.g., depletion zone). Finer elements in general will be needed where the most power dissipation is simulated and where quantities are rapidly changing as a function of location (e.g., interfaces, sharp corners, etc.). This is where the gradients are the largest and the largest errors are committed. A simple method for estimating what is "good enough" is to halve the number of domains or elements in a particular power-dissipating region. If it causes a significant change in the predicted results, this is an indication that the model may not have enough resolution for the problem at hand. While there are more mathematically rigorous methods, numerical errors can be usefully estimated in this manner. Similarly modeling should be performed with both best- and worst-case assumptions for the thermal conductivities, dimensions, doping levels, etc. The difference in resulting temperature predictions is a measure of the model assumption errors. Both numerical and assumptional errors should accompany any temperature predictions and accompanying reliability estimates.

Appendix F. MIMCAP Reliability Estimation in GaN Devices

The purpose of this appendix is to show how to compute a failure rate for a product MIMCAP area with a given usage condition. The "effective thickness" concept is employed to describe the defects that dominate the MIMCAP failure rate. It is assumed that a ramp breakdown test is performed on a suitable sample size to characterize the defect density. The full computation of reliability for an example mission is provided here. This approach uses the Frenkel-Poole model of current conduction in a dielectric that fails after passage of a certain charge to breakdown.

F.1 Frenkel-Poole Conduction and Charge to Breakdown Model

By previous characterization, it is assumed that the MIMCAP current-voltage-temperature (IVT) characteristic has been determined. For typical plasma-deposited silicon nitride dielectric films, the current conduction mechanism is by Frenkel-Poole hopping conduction (Hesto, 1986), and this is assumed here. The Frenkel-Poole current density is given by

$$J_{FP} = \sigma E \exp\left[\frac{-\left(\phi_t - \beta\sqrt{E}\right)}{kT}\right] \tag{F-1}$$

where σ is the Frenkel-Poole conductivity, E is the electric field, ϕ_t is the trap depth below the conduction band, β is the Frenkel-Poole slope coefficient, k is Boltzmann's constant, and T is absolute temperature. The Frenkel-Poole assumption can be verified observing a linear plot of $\ln(J/E)$ versus $E^{1/2}$. A typical Frenkel-Poole plot is shown in Figure F-1 at room temperature. From the temperature dependence, the trap depth parameter ϕ_t can be determined. The IVT characterization should be performed in the dark on reasonably large-sized capacitors devoid of additional conducting traces, bondpads, or other leakage paths so that the true current conduction in the bulk of the dielectric is revealed. Edge effects can also contribute to additional leakage, and they can be estimated by measurement of MIMCAPs with differing peripheries and subtracted from the bulk currents.

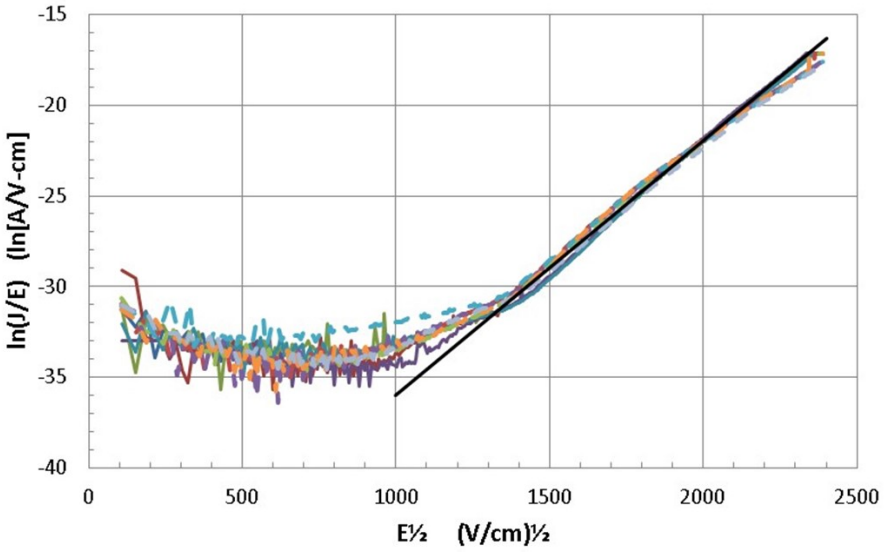


Figure F-1. Frenkel-Poole plot of a Si_3N_4 MIMCAP with insulator thickness of approximately 250 nm. The Frenkel-Poole characteristic straight line is shown at higher fields above the noise floor for the current measurement, approximately 1 nA.

In an amorphous insulator, the bandgap energy is large (for example approximately 5 eV for Si_3N_4) and the carrier densities are extremely low. However, because of the amorphous nature of the dielectric film, there are missing or dangling bonds, stretched bonds, and vacancies throughout the film that manifest themselves as traps. The Frenkel-Poole conduction mechanism is attributed to electrons hopping from trap to trap under the influence of an applied electric field. The theory applies when the trap is neutral while an electron is trapped and becomes positively charged when the electron escapes. Such a trap having a coulombic potential well with trap depth ϕ_t is shown in Figure F-2. With no applied electric field, the potential well is symmetrical, and the probability of emission of a trapped electron into the conduction band is assumed to be Maxwellian and proportional to $\exp(-\phi_t/kT)$. When an external electric field is present, the coulombic potential well becomes distorted as shown, and the barrier is lowered by an amount $\Delta\phi$ on the downstream side. The Frenkel-Poole derivation (Ongaro, 1992) provides the relationship between the barrier lowering and the applied electric field E as

$$\Delta\varphi = \sqrt{\frac{q}{\pi\varepsilon_0\kappa}} \times E^{1/2} \tag{F-2}$$

where q is the electronic charge, ε_0 is the permittivity of free space, and κ is the dielectric constant. The constant term under the square root is sometimes called the Frenkel-Poole field-lowering coefficient or the Frenkel-Poole emission coefficient and denoted by $\beta = \sqrt{q/\pi\varepsilon_0\kappa}$. With the lowered barrier, the emission probability of a trapped electron now becomes much larger and is proportional to $\exp(-(\phi_t - \beta E^{1/2})/kT)$. The original Frenkel-Poole derivation suggests using the optical dielectric constant here rather than the conventional dielectric constant. This is because the interaction of the trap with the electron involves very short times and short ranges that are much faster and more confined than the usual dielectric relaxation time and long-range electrostatic interaction distances. For example, the conventional dielectric constant of Si_3N_4 is about 7.5, while its optical dielectric constant is approximately 4. This coefficient β provides the slope of the Frenkel-Poole curve, and from the linear fit in Figure F-1 we find in fact that $\kappa = 4.4$.

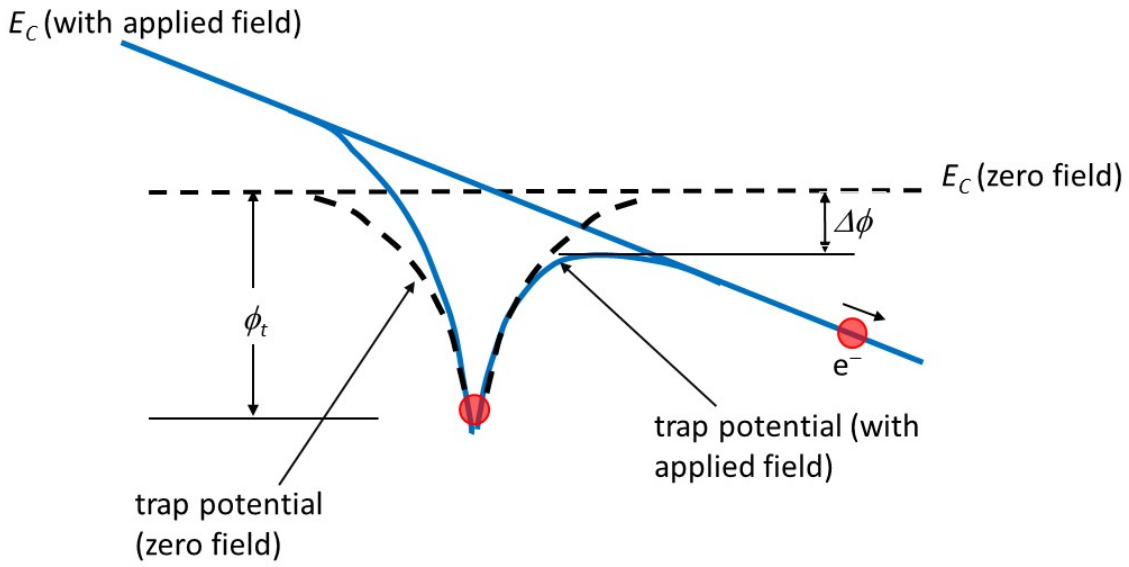


Figure F-2. Frenkel-Poole current conduction model for an amorphous insulator. The conduction band energy E_C is shown with both zero field (dotted line) and with an applied field (solid line). The conduction band is modified by the presence of a coulombic trap potential profile of depth ϕ_t in both cases. In the presence of an applied electric field the coulombic potential barrier is lowered by an amount $\Delta\phi$ on the downstream side, increasing the probability of emission of the trapped electron (red dot).

When the electric field is very high, such that $\beta E^{1/2} > \phi_t$, the Frenkel-Poole model no longer is an accurate representation of the physical situation. In the high field case, the barrier lowering is so extreme that essentially all the electrons are de-trapped and move through the conduction band unimpeded. The exponential term in the Frenkel-Poole expression is then no longer applicable, and the conduction of current in the dielectric becomes temperature independent. The vanishing of the temperature coefficient of current is in fact observed in Si_3N_4 at sufficiently high field (Harrel, 1999). Beyond this condition, all the traps are exhausted of electrons—this is termed the "exhaustion mode." The exhausted current density (in Harrel, 1996, the term "saturation" is used but is avoided here lest it be confused with a saturated HEMT current) then becomes simply

$$J_{exh} = \sigma E \tag{F-3}$$

The "complete" expression for the current density is then

$$J_c\left(V, x_{eff}, T\right) = \begin{cases} \sigma \dfrac{V}{x_{eff}} \exp\left[\dfrac{-\left(\varphi_t - \beta\sqrt{V/x_{eff}}\right)}{kT}\right] & \text{if } \dfrac{V}{x_{eff}} < \dfrac{\varphi_t^2}{\beta^2} \\ \sigma \dfrac{V}{x_{eff}} & \text{otherwise (exhaustion)} \end{cases} \tag{F-4}$$

So far, conduction has been described by electrons de-trapped from neutral donor centers (neutral donor traps losing an electron and becoming positively charged). However, conduction could be equally well described by holes de-trapped from neutral acceptor centers (neutral acceptor traps losing a hole and becoming negatively charged). It has not been definitively established whether conduction in Si_3N_4 is by holes or electrons.

F.2 Example MIMCAP

An example MIMCAP that might be found in a typical GaN fabrication process is now postulated for the purposes of demonstrating the calculating of reliability (Scarpulla, 1999 & 2011). For this example case the nitride is assumed to have the following properties:

$x_0 = 300$ nm	nominal thickness
$C = 220$ pF/mm^2	nominal capacitance
$\sigma = 2 \times 10^{-8}$ S/cm	Frenkel-Poole conductivity coefficient
$\phi_t = 1.1$ eV	trapping depth or activation energy
$\beta = 3.62 \times 10^{-4}$ cm$^{1/2}$V$^{1/2}$	Frenkel-Poole emission coefficient
$Q_{BD} = 1.5$ Coul/cm^2	charge-to-breakdown

Also, it is convenient here to specify sundry other parameters for later analysis that ultimately define the reliability of this MIMCAP in a typical space mission.

$t_m = 15$ years	usage or mission time
$T_m = 150$ °C	usage or mission temperature
$R = 5$ V/sec	ramp rate for breakdown test
$A_t = 0.1$ mm^2 (335 μm × 300 μm)	area of test capacitors
$A_p = 0.015$ mm^2	area of product capacitors

F.3 Charge-to-Breakdown

It is also assumed by previous characterization that the charge-to-breakdown Q_{BD} has been established for the dielectric. The time-dependent dielectric breakdown theory is based upon the concept of an accumulated damage that may be accelerated with elevated temperature and field. The current density provides this damage. When a certain charge has flowed through the dielectric, the condition for failure is reached. The charge-to-breakdown is assumed in this example to be 1.5 Coul/cm^2 and constant, being independent of temperature. This is lower than that in some GaAs processes surveyed recently (Scarpulla, 2011), primarily to better fit preliminary data in a GaN process. In practice, relatively small-area capacitors should be stressed at elevated temperature to quantify the charge to breakdown of the MIMCAP dielectric. Small-area MIMCAPs tend to have fewer extrinsic defects, and thus the true charge to breakdown of the intrinsic dielectric can be measured. The charge to breakdown is the time integral of the current density

$$\begin{aligned} Q_{BD} &= \int_0^{t_F} J\left(E(t), T(t)\right) dt \\ &= J(E,T)\, t_F \end{aligned} \tag{F-5}$$

Since both the temperature and/or electric field may vary in time, their explicit time dependence is included in the upper integral expression, whereas if temperature and electric field are constant, the integral simplifies to the lower algebraic form.

F.4 Effective Thickness Concept

Next the concept of an effective thickness is postulated (Scarpulla, 1999). It is assumed that the dielectric is mostly uniform with nominal thickness x_0. The nominal electric field is $E_0 = V/x_0$, where V is the applied voltage to the MIMCAP. However, there are places or spots within the area of the dielectric

where defects exist, either physical ones (for example a metal particle), or electrical ones (such as a weak bonding arrangement in one spot). Defective spots are very small in area compared to the main area of the dielectric, and thus are undetectable physically or electrically until failure occurs. They are characterized by a range of effective thicknesses x_{eff} that varies from the nominal thickness down to zero. The electric field at these weak spots is

$$E = V/x_{eff,} \tag{F-6}$$

and may be much higher than the nominal electric field.

In a MIMCAP with a constant applied voltage and temperature, the defect spots where $x_{eff} < x_0$ have a higher electric field and a higher current density and reach the charge-to-breakdown condition sooner than in the nominal part of the dielectric. In fact, the weakest link breaks down first. These weakest links dominate the reliability rather than the main portion of the dielectric. For a constant temperature, and constant voltage test condition (or for a typical application in a MMIC where temperature and applied voltage are constant), the total charge conducted over a time t is given by

$$\begin{aligned} Q &= \frac{t\sigma V}{x_{eff}} \exp\left(-\frac{\left(\phi_t - \beta\sqrt{V/x_{eff}}\right)}{kT} \right) \quad \text{if } x_{eff} > \frac{\beta^2}{\phi_t^2} V \\ &= \frac{t\sigma V}{x_{eff}} \qquad \text{otherwise (exhaustion)} \end{aligned} \tag{F-7}$$

where the Frenkel-Poole condition applies for low fields when x_{eff} is large, and the trap exhaustion temperature-independent condition applies for larger fields. The demarcation between these regimes is the exhaustion condition

$$x_{ex} = \frac{\beta^2}{\phi_t^2} V_{ex} \tag{F-8}$$

For the example MIMCAP with a constant applied usage voltage V = 40 V, exhaustion occurs below x_{ex} = 43.3 nm. Any defects having an effective thickness smaller than this x_{ex} will conduct all available trapped electrons, will develop the charge to breakdown relatively quickly, and will have a short lifetime. The times to breakdown t_{BD} for various values of x_{eff} are plotted in Figure F-3. The range of times in this plot extends over 13 decades. The exhaustion condition at very small effective thicknesses corresponds to high fields and extremely short lifetimes. These small effective thicknesses are at the very worst defects in the MIMCAP. For effective thicknesses close to the nominal thickness of 300 nm, the lifetimes are $>10^9$ hours. A plot like this can be developed for any set of constant conditions (temperature, voltage, etc.) to determine MIIMCAP lifetime.

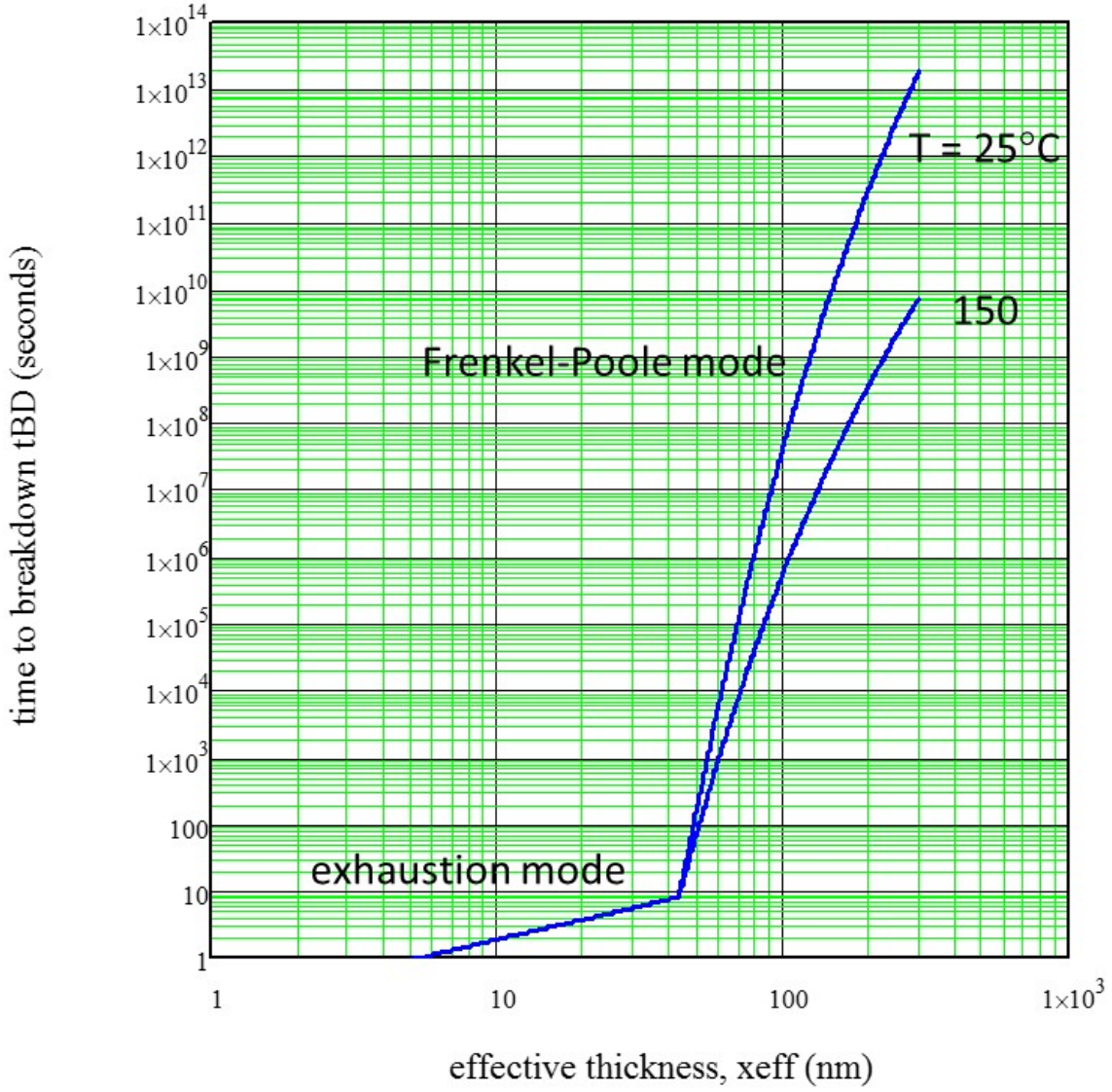


Figure F-3. Times to breakdown under constant voltage conditions of $V = 40$ V for the example MIMCAP versus effective thickness for two temperatures using the Frenkel-Poole model. Note the extremely large range of the times to breakdown.

F.5 Determination of Defect Density

Clearly the defects as described by small values of x_{eff} would be detrimental to reliability if they were prevalent. The next undertaking is to extract MIMCAP defect densities so as to determine reliability. If our example MIMCAP was to fly in a space mission having a duration of $t = 15$ years, at a constant applied voltage of 40 V and temperature of 150 °C, how large must x_{eff} be in order to assure an acceptable failure rate? Every semiconductor process contains some degree of defects—what density of what x_{eff} values is tolerable to achieve the desired reliability in the example MIMCAP in a space mission? In order to obtain this information, a ramp breakdown test is performed on a large sample of test MIMCAPs, each of area A_t. For our example case, the voltage is ramped at a rate of $R = 5$ V/sec at room temperature and the test capacitor areas are $A_t = 0.1$ mm^2. Instead of observing a time to breakdown, the breakdown voltage V_{BD} during the ramp is recorded for each sample. The objective is to extract a x_{eff} value from each

sample breakdown voltage. Since voltage is no longer constant, the integral form of the charge-to-breakdown expression must now be used. The ramp voltage on the test capacitor is $V(t) = Rt$, and substituting this into the above integral along with the Frenkel-Poole current density, the charge conducted as the voltage is ramped to voltage V is

$$Q_{FP}\left(V, x_{eff}\right) = \int_0^{V_{BD}} \frac{\sigma V}{x_{eff} R} \exp\left(-\frac{\left[\phi_t - \beta\sqrt{V/x_{eff}}\right]}{kT} \right) dV \equiv Q_{BD} \tag{F-9}$$

A simplifying assumption is that the charge-to-breakdown Q_{BD} is constant for any effective thickness x_{eff}. This assumption allows an observed ramped breakdown voltage V_{BD} to be related directly to an effective thickness. To do this, the above integral must be solved. While it can be solved analytically, the result is complex. A numerical solution is simple to implement and describe. To solve this numerically, an effective thickness is first chosen. Effective thicknesses should be varied from zero up to the nominal dielectric thickness or slightly thicker. For each effective thickness chosen, the integral is performed numerically to find the charge passed through the dielectric as the applied voltage ramps up. The integration is approximated by a sum of a series of small voltage steps. The integral is started from 0 volts and proceeds until the charge reaches the charge-to-breakdown, thus determining the breakdown voltage for the selected x_{eff}. However, if the exhaustion voltage condition

$$V_{ex} = \frac{\phi_t^2}{\beta^2} x_{ex} \tag{F-10}$$

is reached before the charge-to-breakdown condition is achieved, the integrand is changed midstream to the simpler $\sigma V/x_{eff} R$ (the exponential is dropped) and the process continued. Figure F-4 shows the breakdown voltages computed in this manner for various effective thicknesses in the example MIMCAP. Note that the temperature dependence of the curves is small, as indicated by the small difference between breakdown voltages at 25 °C versus 150 °C. This comes about because as the voltage ramps up toward breakdown, much of the charge to breakdown is developed in the last few voltage steps in the exhaustion mode, which is temperature independent. Using the table look-up plotted in Figure F-4 (indicated as exact), any ramped breakdown voltage may be converted into a corresponding effective thickness.

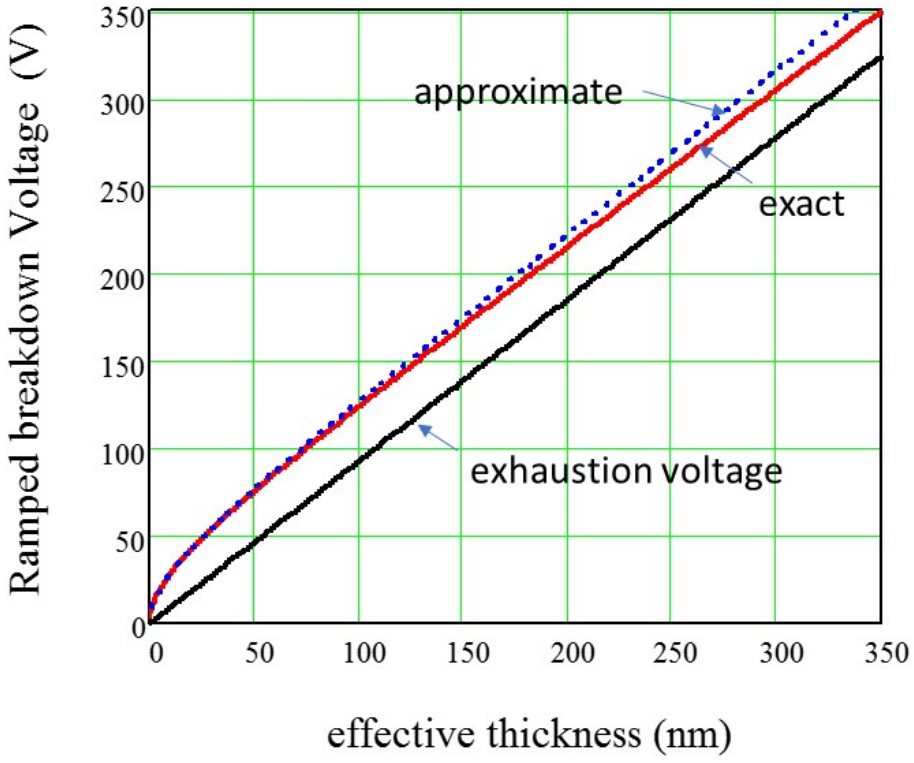


Figure F-4. Predicted ramped breakdown voltage for assumed effective thicknesses up to 350 nm. Both the exact (solid line) and approximate (dotted line) breakdown voltages are shown for room temperature and a ramp rate of 5 V/sec. The exhaustion voltage is also shown for comparison.

For reference, Figure F-4 also shows the exhaustion voltage for the various effective thicknesses assumed in the example MIMCAP. If only the exhaustion current is included in the integral of Eq. (F-9), it simplifies to

$$Q_{ex} = \int_{V_{ex}}^{V_{BD}} \frac{\sigma}{Rx_{eff}} V dV = \frac{\sigma}{2Rx_{eff}} \left(V_{BD}^2 - V_{ex}^2 \right) \tag{F-11}$$

where the integral covers the voltage range only from V_{ex} to V_{BD}. Solving for V_{BD} gives the approximation

$$V_{BD} \approx \sqrt{\frac{2x_{eff} RQ_{BD}}{\sigma} + V_{ex}^2} \tag{F-12}$$

This exhaustion-only approximation is also plotted on Figure F-4 (dotted line) for comparison. The approximation predicts a slightly higher breakdown voltage than the numerical solutions. This is not surprising since the approximation lacks some of the current contributed during the ramp-up from zero. Nevertheless, it is a simple and useful analytic approximation to the numerical solution.

Figure F-4 is interpreted as follows. Suppose the example MIMCAP has a defect with an effective thickness of 150 nm, exactly half of the nominal thickness. The exhaustion voltage is about 140 V. If a voltage of 140 V or greater is applied, all traps are emptied, and the current becomes temperature-independent, no longer controlled by hopping conduction. The approximation of Eq. (F-12) is the voltage

reached during the ramp up (with a rate 5 V/sec in this example) when Frenkel-Poole hopping conduction is completely ignored. In other words, in the ramp-up between 0 V and 140 V, no current at all is assumed to flow in the MIMCAP. Upon reaching the exhaustion voltage of 140 V, the current then begins to flow. As the ramp proceeds beyond 140 V, more and more current flows, eventually accumulating the necessary charge-to-breakdown Q_{BD}, reached at about 175 V (dotted line approximation in Figure F-4). Actually, including the Frenkel-Poole current contribution in the ramp-up below 140 V gives the more exact solution (solid line in Figure F-4), which is just slightly lower than 175 V. It is lower because including the additional Frenkel-Poole current causes the charge-to-breakdown to be achieved slightly earlier in the ramp. Note also that the approximate solution is temperature independent, while the exact solution contains the temperature dependence of the Frenkel-Poole conduction model during the ramp-up to V_{ex}.

The next step is to determine the density of defects, ultimately determining the reliability of the MIMCAP. A MIMCAP ramped breakdown voltage (or a set of breakdown voltages) indicates the effective thickness of its weakest defect (or set of defects). A table look-up of the numerical solution provides an accurate mapping from the measured ramped breakdown voltage to the effective thickness of the defect it indicates. On the other hand, the effective thickness can be estimated from the exhaustion approximation by solving a quadratic for x_{eff}:

$$\frac{\varphi_t^4}{\beta^4} x_{eff}^2 + \frac{2RQ_{BD}}{\sigma} x_{eff} - V_{BD}^2 = 0 \qquad \text{(F-13)}$$

This is the solution of approximation (F-12) after substituting for V_{ex}. In this way the observed breakdown voltages during the ramp test may be converted into approximate effective thicknesses in lieu of the exact integration table look-up.

Figure F-5 shows a normal probability plot of a set of ramped breakdown voltages from 496 test samples across multiple wafers. The majority of the samples break down at a reasonably high voltage well above about 250 V. This particular tester is limited to a maximum voltage of 300 V and a sizable fraction of about 40% of MIMCAPs did not break down and are plotted at this maximum voltage. This is not a limitation since the subset having lower breakdown voltages, as evidenced by the lower tail on the probability plot, are the key to the reliability calculation. This tail of the distribution contains the information needed to extract the reliability of the MIMCAP in usage. The probability scale shown is for a normal distribution and is for plotting purposes only—the data is clearly not from a normal distribution. The probabilities shown on this plot can be converted into defect densities using a defect model.

First, however, it is recommended that a simple sanity check be performed on the MIMCAP model using Eq. (F-13). Substituting the maximum (or alternatively the 95th percentile) of the breakdown voltages from a plot such as Figure F-5 and solving Eq. (F-13) should yield an effective thickness very close to the nominal nitride thickness. This provides some confidence that the model parameters (β, σ, ϕ_t, and Q_{BD}) are reasonably correct. In Figure F-5 this is not quite possible because the 95th percentile of the breakdown voltage distribution is not observable because of test equipment limitations. In this case, the breakdown voltages are observable only up to about the 60th percentile at 300 V. At this point, the breakdown condition is well into the intrinsic breakdown region. The 300 V breakdown value gives an effective thickness of x_{eff} = 295 nm. This is reasonable because it is quite close to the nominal nitride thickness.

It is strongly recommended that this sanity check be performed on the MIMCAP model parameters. The example parameters here were chosen based upon one particular MIMCAP process. Other MIMCAP processes may yield very different values. In a survey of many different MIMCAPs from many

fabrication lines (Scarpulla, 2011), the ranges of the four Frenkel-Poole conduction model parameters were as follows:

β	2×10^{-4} to 5×10^{-4}	Frenkel-Poole emission coefficient ($cm^{1/2}V^{1/2}$)
σ	7×10^{-9} to 1×10^{-3}	Frenkel-Poole conductivity (S/cm)
ϕ_t	0.7 to 1.1	trap depth (eV)
Q_{BD}	5 to 150	charge to breakdown (Coul/cm^2)

The ranges of these parameters are large owing to the many differences in processing conditions possible. The Frenkel-Poole conductivity varies widely—it will then have a large impact on the ramped breakdown voltage. The trap depth also varies in that it will change the degree of the temperature dependence of the reliability. It is very important to independently characterize these parameters with small test capacitors to obtain the Frenkel-Poole conduction properties (see Frenkel-Poole plot of Figure F-1).

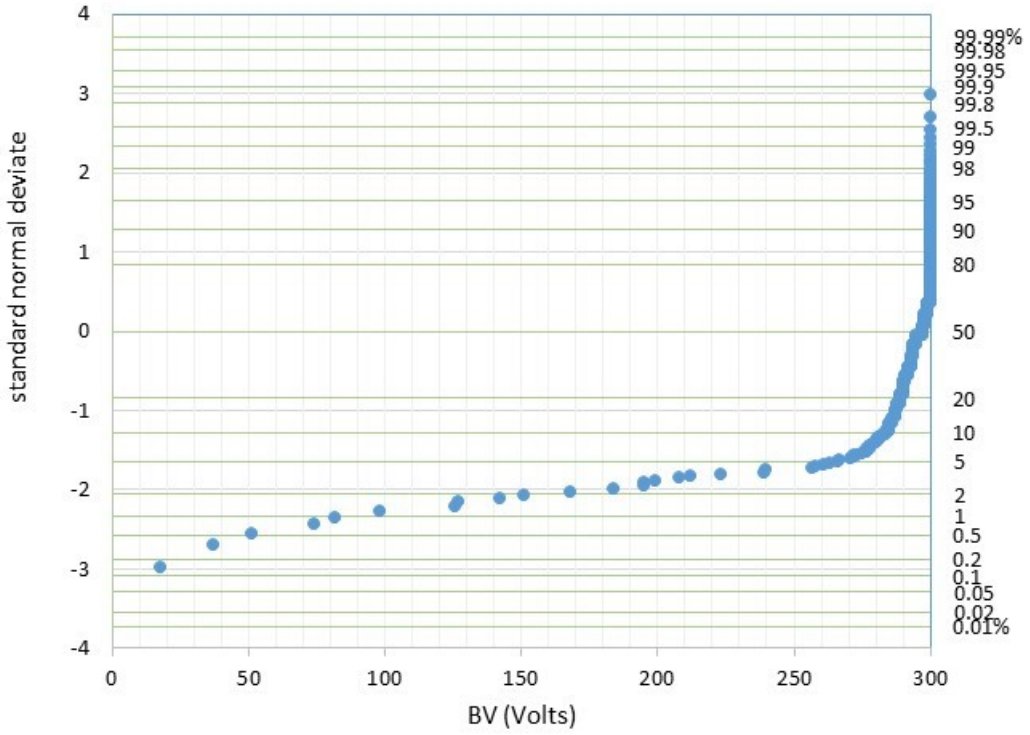


Figure F-5. Normal probability plot of ramped breakdown voltages of a set of MIMCAPs of area 0.1 mm^2, at room temperature and with ramp rate 5 V/sec.

The simplest model to describe defects is the Seeds yield model (Seeds, 1967) given by

$$Y = \left(1 - P_f\right) = \frac{1}{1 + DA_t} \tag{F-14}$$

which was originally proposed to predict the yield of an integrated circuit with active area A_t built in a fabrication process having defect density D. It is a simplification of the Poisson yield model and for relatively low defect densities is virtually identical. Its advantage lies in the fact that it is simpler algebraically than the Poisson model. The yield in this context can be interpreted as $1 - P_f$, where P_f is the probability taken from the ramped breakdown failure voltages, to wit, the probability from Figure F-5.

The Seeds model can be rewritten so as to extract the cumulative defect densities directly from the probabilities P_f as

$$D = \frac{1}{A_t}\frac{P_f}{1-P_f} \tag{F-15}$$

This allows the transformation of the probability scale of Figure F-5 into the defect densities. Accompanying this transformation is the conversion of ramped breakdown voltages into the effective thicknesses using the exact table look-up described above in Figure F-4.

In this way the probability plot of Figure F-5 can be transformed into a plot of defect density vs. effective thickness. The transformation process is

$$\begin{aligned} P_f &\rightarrow D \\ BV &\rightarrow x_{eff} \end{aligned} \tag{F-16}$$

The defect densities have units of area^{-1} and are cumulative defect densities because the probabilities P_f are cumulative failure probabilities. Making this transformation of the data of Figure F-5 gives the plot of Figure F-6. Its interpretation is as follows: for each particular x_{eff} value on the plot, there are D cumulative defects per unit area having that x_{eff} or less. The cumulative defect density tends toward large numbers for large effective thicknesses. This is because of the fact that the entire quantity of N MIMCAPs subjected to a ramped breakdown test will be enveloped if x_{eff} is sufficiently large. In fact, the largest computed value of the defect density for a given sample size N of test MIMCAPs each with area A_t is approximately N/A_t. Similarly, the smallest defect density that can be captured is approximately $1/NA_t$. It behooves the user to use a large sample size of large MIMCAPs to obtain the greatest sensitivity in measuring the defect density of a MIMCAP process. Also note that in Figure F-6 the largest effective thicknesses extracted are at approximately x_{eff} = 295 nm, corresponding to the largest achievable ramped voltage of 300 V. Had the test equipment been capable of higher voltages, the upper range of this curve would have extended toward higher values of x_{eff}, quite possibly beyond the nominal thickness of x_0 = 300 nm. Values slightly larger than x_0 are always possible due to process thickness variations.

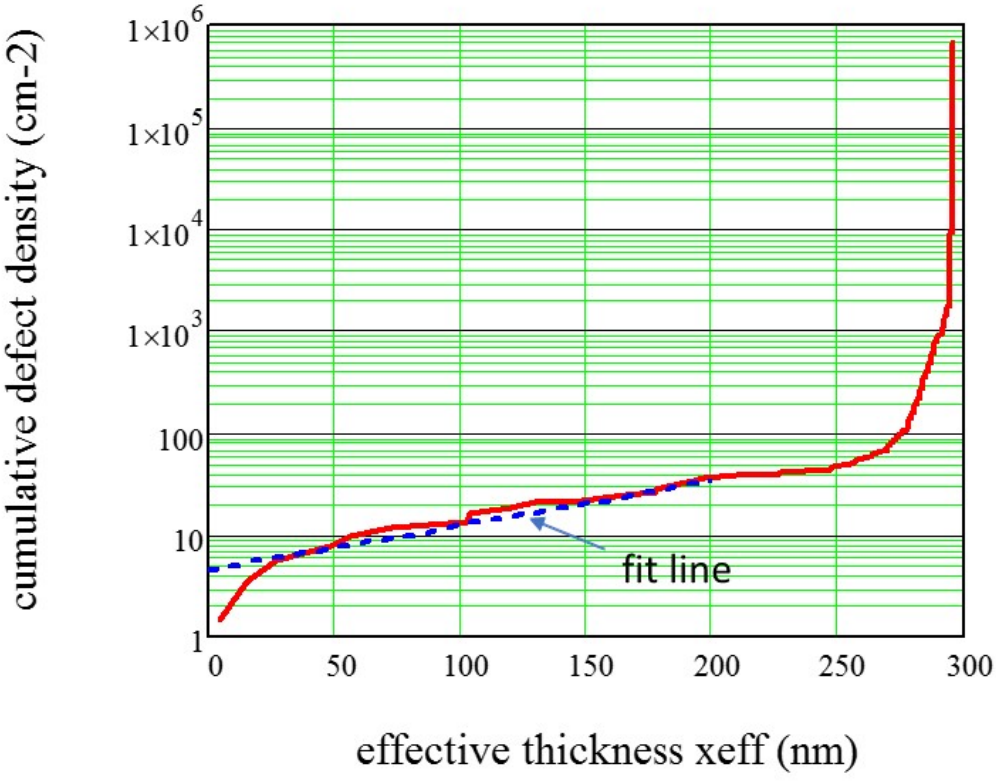


Figure F-6. Cumulative defect density vs. effective thickness. This is the transformation of the data of Fig. F-5 using the Frenkel-Poole model.

It is convenient to approximate the tail of the D vs. x_{eff} characteristic (Figure F-6) with a simple curve fit model. A typical fitting function is of the form

$$D = D_0 \exp\left(\frac{x_{eff}}{x_C}\right) \tag{F-17}$$

where D_0 is the defect density extrapolated to zero effective thickness, and x_C is a characteristic effective thickness. On a semi-log plot such as Figure F-6, D_0 is the intercept and x_C^{-1} is the slope. The parameters of the fit line displayed in Figure F-6 are $D_0 = 4.5$ defects/cm^2 and $x_C = 100$ nm.

F.6 MIMCAP Reliability

Now that the defect density characteristic of the process has been determined, it remains to show a typical MIMCAP reliability calculation. The MIMCAP will be assumed to be used in a space mission, but first it is subjected to a short, elevated-voltage screen at the factory, followed by a burn-in at elevated temperature in the user's assembled module, and finally followed by the mission itself. The sequence of these various phases, their durations, and the conditions are shown in Table F-1. As the MIMCAP proceeds through the screen and burn-in, defects are removed up to the effective thicknesses shown in the table. During the mission, the defects that remain behind contribute to the ultimate failure rate. To calculate the effective thicknesses first removed by the screen, an iterative calculation is performed on x_{eff} of the function

$$Q_{BD} - J_c\left(V_s, x_{eff}, T_s\right) \times t_s = 0 \tag{F-18}$$

where the "complete" current density expression (F-4) is used here. It switches to the exhaustion mode when the conditions demand it. The other quantities V_s, T_s, and t_s are the voltage, temperature, and time duration of the screen, respectively, as defined in Table F-1. The first term of Eq. (F-18) is the charge-to-breakdown constant, while the second is the charge passed through the MIMCAP over the screen time. They must balance to zero. Finding the root of this function gives the effective thickness up to which defects are removed by the screen. Note that the simple exhaustion approximation made with respect to the ramp breakdown test is usually not valid here. The Frenkel-Poole current density is usually predominant unless the screen voltage is very high.

Table F-1. Three phases in the life of a MIMCAP—screening, burn-in, and the mission. The durations, temperatures, and voltage conditions of each phase are shown along with the effective thicknesses and defect densities terminating each phase using the Frenkel-Poole model. The absolute and conditional probabilities for each phase are tabulated, and the mission failure rate can then be calculated from the mission conditional failure probability.

phase	duration	voltage	temper-ature	*Effective thickness*, x_{eff} (nm)	*Cumlative defect density* (defects/ cm^2)	absolute failure probability	conditional failure probability
screen	60 sec.	60V	25°C	71.1	11.4	0.171%	–
burn-in	320 hrs	40V	150°C	106.7	16.2	0.242%	0.071%
mission	15 yrs.	40V	90°C	155.7	29.0	0.343%	0.101%
				Mission average failure rate, AFR			7.7 FITs

The next phase of the life of the MIMCAP is a burn-in at elevated temperature at usage voltage conditions. The root for x_{eff} of the expression

$$Q_{BD} - J_c\left(V_s, x_{eff}, T_s\right) \times t_s - J_c\left(V_b, x_{eff}, T_b\right) \times t_b = 0 \tag{F-19}$$

is now used to find that x_{eff} value for which defects are removed by the end of the burn-in. The second term contains the quantities V_b, T_b, and t_b that are the voltage, temperature, and time duration of the burn-in respectively as defined in Table F-1. In this expression x_{eff} appears twice—both in the screen and the burn-in charge terms. This happens because charge passed through the MIMCAP in the screen adds to the charge in burn-in, and their sum must balance the charge-to-breakdown constant. Finally, for the long-duration mission, a similar root must be found for x_{eff} in

$$Q_{BD} - J_c\left(V_s, x_{eff}, T_s\right) \times t_s - J_c\left(V_b, x_{eff}, T_b\right) \times t_b + J_c\left(V_m, x_{eff}, T_m\right) \times t_m = 0 \tag{F-20}$$

where V_m, T_m, and t_m are the voltage, temperature, and time duration of the mission. Now there are three charge terms to balance the charge-to-breakdown constant. This process can be repeated for as many phases of MIMCAP life needed. For example, there may be other test or ground operational phases to add in, or there may be different phases during the mission, for example, mission phases where the voltage or temperature might be differing. All these can be accommodated using the approach of adding the charge

terms and finding the x_{eff} root. The mission time t_m in the above expression may be treated as a variable, swept from the beginning of the mission at $t_m = 0$ to the end of the mission. This gives a look at how the probability of failure and failure rate vary as the mission proceeds. A decreasing failure rate is usually observed.

Now that the effective thicknesses in the example MIMCAP corresponding to the screen, the burn-in and the mission have been determined, as shown in Table F-1, it is possible to derive the failure rate. The desired failure rate is the conditional failure rate during the mission, given that the MIMCAP has successfully passed the screen and burn-in. First the defect densities are extracted by interpolation of the data of Figure F-6 (or using the fitted curve). For the example MIMCAP, these densities are shown in Table F-1 using the interpolated version.

Next the absolute probabilities of failure are found from the Seeds model, for example, for the probability of screen failure as follows

$$P_s = \frac{D_s A_p}{1 + D_s A_p} \tag{F-21}$$

where D_s is the defect density for that x_{eff} found at the end of the screen, and similarly for the burn-in, and mission probabilities P_b and P_m.

$$P_b = \frac{D_b A_p}{1 + D_b A_p} \quad \text{and} \quad P_m = \frac{D_m A_p}{1 + D_m A_p} \tag{F-22}$$

The MIMCAP area to use here is A_p—the area of the product MIMCAP—rather than that of the test capacitors used in the ramp breakdown test. These three probabilities are shown in Table F-1. They are absolute probabilities. This means that they describe the probability of failing the screen, failing the combined screen plus burn-in, and failing the combined screen plus burn-in plus mission. Rather than absolute probabilities, the conditional probabilities are more useful and are

$$P_{cb} = \frac{P_b - P_s}{1 - P_s} \quad \text{and} \quad P_{cm} = \frac{P_m - P_b}{1 - P_b} \tag{F-23}$$

giving P_{cb}, the conditional probability of failing the burn-in having passed the screen, and P_{cm}, the conditional probability of failing the mission having passed both the screen and burn-in. These conditional failure probabilities are shown in the final column of Table F-1.

The final step is to obtain the mission failure rate for the example MIMCAP as

$$\lambda = -\frac{\ln(1 - P_{cm})}{t_m} \times 10^9 \quad [\text{FITs with } t_m \text{ in hours}] \tag{F-24}$$

This is actually an average failure rate, not the instantaneous hazard rate. It is the failure rate averaged over the entire mission. By sweeping the time t_m incrementally from the beginning to end of the mission and stepping through the calculations for each, it is possible to generate a running average failure rate versus time. This is shown in Figure F-7. For the calculations using the interpolation of the defect density data of Figure F-6, the final failure rate at mission's end is 7.7 FITs. Using the curve fit for the defect densities it is 9.4 FITs. The agreement between the two is good in Figure F-7. The earliest mission times

have a larger discrepancy due to the deviation of the curve fit from the somewhat unsmooth data in Figure F-6.

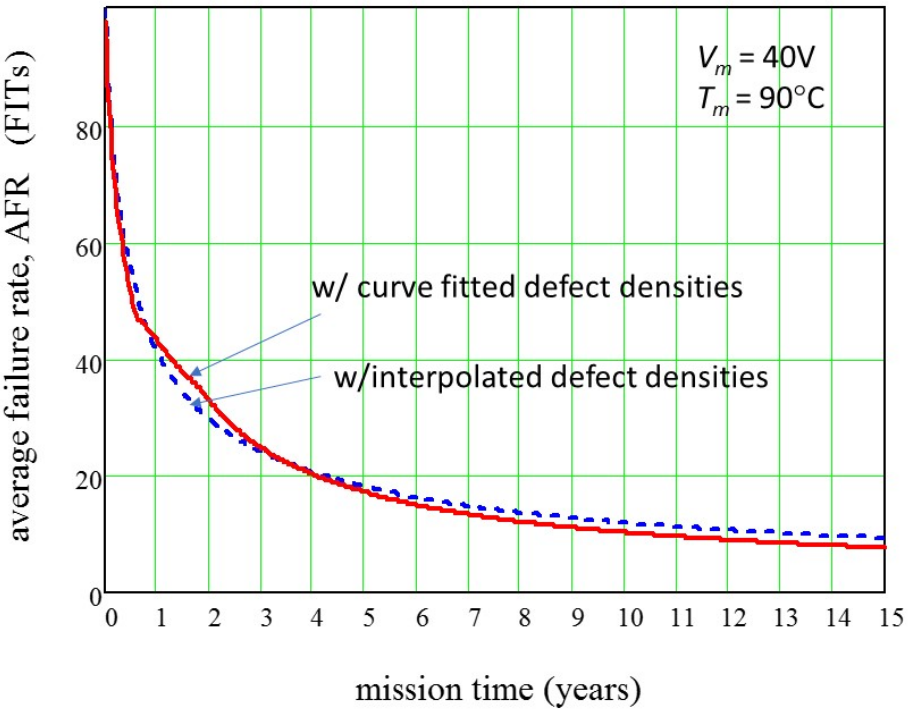


Figure F-7. Average failure rates for the interpolated and curve-fitted defect densities during a 15-year mission using the Frenkel-Poole model.

F.7 Discussion

While the example MIMCAP analysis provided above utilizes the Frenkel-Poole conduction approach, other models of dielectric breakdown have been proposed, for example, the bond-breaking model (E-model) or the Fowler-Nordheim tunneling model (1/E) model. It has been stated in the past that these may be more conservative. However, this may not be a correct statement in the context of the relatively thick MIMCAP dielectrics that are found in GaN MMICs. The E- or 1/E-models predict smaller times to fail for very high fields. So, when extrapolating to normal usage electric fields, the times to fail are generally believed to be more conservative. High fields, too, are associated with the defects having small x_{eff} values even at normal usage voltages and temperatures. Therefore, the benefits of screening and burn-in may be overestimated, since the defects are given shorter times to fail by the E- or 1/E models. In other words, for a given screen or burn-in, removal of more defects by the E- or 1/E models may be predicted than actually occur. Then during the mission life, the density of remaining defects may actually be higher than anticipated, giving a poorer mission reliability. Therefore, it is recommended here to utilize the Frenkel-Poole/charge-to-breakdown model since it predicts a more conservative actual post-burn-in reliability.

It is sometimes stated that the low activation energy observed for breakdown voltage is an indicator that tunneling is the governing mechanism. However, it is seen in the example calculation that this is not the case. Trap exhaustion contributes most of the charge to breakdown and is essentially temperature independent. Therefore, the low activation energy does not necessarily discount the Frenkel-Poole conduction model. At normal usage voltages, the MIMCAP remains in the Frenkel-Poole conduction mode with a strong temperature dependence. However, in the ramp breakdown voltage test mode, the

MIMCAP will enter trap exhaustion, and the temperature dependence of the breakdown voltage essentially vanishes. This lack of temperature dependence does not imply a tunneling mechanism and may argue against the E or 1/E models that have very small thermal activation energies.

It is also recommended that the selection of models for time-dependent breakdown be approached with care, and to choose the correct model based upon the physics of the phenomenon. All models are approximations of the true physical conditions that cause failure in MIMCAPs and are greatly simplified. For example, rather than a single trapping level in the Frenkel-Poole model, there may be a distribution or range of trap energy levels, making the situation much more complex. In the E-model, the bonds that are broken that eventually create the dielectric failure have a distribution of bond lengths and angles, and so the field coefficient might be expected to have a distribution of different values. To try to correct these deficiencies might lead to better models at the expense of greater complexity.

In the Frenkel-Poole example cases above, it has been assumed that only Frenkel-Poole conduction occurs, to the exclusion of other current conduction mechanisms. It is possible that at different regimes of the electric field, different current conduction modes may dominate. For example, at lower electric fields, there may be a bulk conduction mode that is nearly ohmic, possibly controlled by the shallower traps that are exhausted at higher fields. At very high fields, space charge conduction may occur. For the sake of simplicity in illustration, it has been assumed above that the Frenkel-Poole mode is the only important one, or at least the only one for which charge accumulation to Q_{BD} is important. This assumption may not be true, and additional model complexity and testing may be warranted by the addition of different conduction modes.

It should also be pointed out that to assess the defect densities of MIMCAP dielectric in a GaN fabrication process, the test capacitor itself should be sufficiently large. Further, the sample size must be sufficiently large. It is recommended that the total MIMCAP area devoted to ramp breakdown testing of NA_t be at least 1,000× the product MIMCAP area A_p

$$\frac{NA_t}{A_p} > 1{,}000 \tag{F-25}$$

In the example case described above, the test capacitors have an area of $A_t = 0.1$ mm^2 (335 µm × 300 µm) and there are approximately 500 used in collecting the example data. The total dielectric area tested is approximately 50 mm^2. The minimum example defect density that can be detected is therefore roughly $1/NA_t = 2 \times 10^{-2}$ defects per mm^2 or 2 defects/cm^2. The area of the example product is 0.015 mm^2. The ratio of the total tested area to the product area is 3,333, which exceeds the recommendation by a factor of 3.3.

Appendix G. Supplemental GaN Radiation Topics

This appendix contains major contributions from Joe Srour, The Aerospace Corporation.

This appendix presents supplemental information related to the radiation testing of GaN devices for space applications. Most of the traditional radiation standards, analysis methods, and test practices were developed in the ’70s and ’80s in the Si era. Now that GaN technology has emerged in the ’10s and will continue to advance into the ’20s, it is important to understand the space radiation GaN differences that might exist as compared to the traditional Si or GaAs devices.

In this appendix, some basic radiation effects are discussed:

- a comparison of energy deposition in Si and GaN by energetic photons
- a discussion of dose enhancement considerations for GaN devices
- the relative sensitivity of GaN and Si to displacement damage effects
- the interaction of heavy ions with GaN HEMT devices

First a general overview of TID requirements for space is in order.

G.1 General Overview of TID Requirements and Device Testing for Space Applications

Radiation requirements for space programs generally include a TID versus shielding-thickness (*dose-depth*) curve for survivability engineers to use in hardness assurance activities. The shielding thickness is typically expressed in terms of an equivalent thickness of Al, where, to first order, the shielding provided by other materials scales with their density. To determine the dose-depth curve for a given orbit, there are two main steps:

1. Define the radiation environment for that orbit by using currently accepted codes. Only the natural space radiation environment is considered here. For trapped electrons and protons, AE9 and AP9 are used, respectively. For solar particles, ESP/PSYCHIC is used. For galactic cosmic rays, CREME96 is employed. The key primary contributors to the deposition of TID in materials and devices on the spacecraft are trapped electrons, trapped protons, and solar protons. There are secondary contributors as well, with bremsstrahlung being the most important.

2. After defining the radiation environment, all components (i.e., trapped electrons and protons and solar protons) are transported through shielding by typically using the Shieldose-2 code. The output of that process is the TID at each selected shielding thickness that includes the dose due to trapped electrons, trapped protons, and solar protons of all energies and bremsstrahlung xrays. In that manner, the TID vs. shielding thickness curve is fully defined.

Dose-depth information is used in hardness assurance work in the following manner. The first step is to determine what shielding a given electronic part in the system experiences, or “sees.” The most thorough approach involves developing a complete simulation of the entire space vehicle, including all structures, boxes, tanks, cabling, etc. Less-complete simulations are also often used. The simulated space vehicle is then used in conjunction with ray-tracing software to determine the equivalent shielding thickness seen by a given part. That is, many rays extending from that part to outside the space vehicle are examined (e.g., 10,000) in all directions over 4π steradians. All materials and their thicknesses seen along each ray are converted to an equivalent Al thickness. In the end, an equivalent Al shielding thickness is thereby defined for the part of interest. For example, ray tracing might yield a thickness of 250 mils Al. The dose-depth curve then yields the TID that the part in question is predicted to receive on orbit, for example, 50

krad, during the entire mission duration from all sources. It is important to note that the "equivalent" shielding thickness determined from a ray-tracing methodology is not the average of all shielding thickness contributions, but rather the dose that would be received by a spherical shield with the designated equivalent thickness when all contributions are included

The next step in the hardness assurance process is to conduct RLAT. One question is, how does one accurately simulate in ground testing the 50 krad dose the part is expected to receive on-orbit? There are two ways to examine that question. The first is to assume that the device will respond to a 50 krad ionizing dose in the same way regardless of how that dose is deposited. To elaborate, the on-orbit TID is produced by energetic electrons and protons plus bremsstrahlung. In contrast, ground testing is specified to use a Co-60 source in which dose is deposited by secondary electrons produced through Compton scattering of the primary incident photons. Dose is also deposited by the bremsstrahlung produced by those electrons. For numerous common situations and devices, the assumption is valid that one doesn't care how the on-orbit TID is simulated in ground testing.

For Si MOS devices, however, the effectiveness of different incident particles and energies affect the device response in different ways due to the dependence on incident particle type and energy of the recombination of electron-hole pairs produced in silicon dioxide layers. It is the amount of such charge that escapes initial recombination that can contribute to radiation-induced changes in device properties, such as threshold-voltage shifts. Assuming the same applied field strength in the oxide, the amount of escaping charge depends on the incident particle type and energy.

For the types of GaN devices being considered here, insulating layers don't play a primary role in their electrical functionality, so it shouldn't matter how TID is deposited in ground testing. That is, using a Co-60 source to simulate the on-orbit dose is appropriate as long as dose enhancement effects are accounted for (Section G.3).

G.2 Ionizing Dose Deposition Comparisons

The equilibrium total ionizing dose deposited during ground testing depends on the specific material being irradiated (or the device fabricated from that material) and on the radiation source used. Most TID testing is performed using either a Co-60 source or a 10 keV xray irradiator. The deposited dose is most frequently expressed with reference to energy deposition in Si devices, with the most common unit being rad(Si). The rate at which energy is absorbed in photon-irradiated materials depends on material type and photon energy. TID comparisons at a specific photon energy can be made by comparing the mass energy-absorption coefficients for different materials. A Co-60 gamma-ray source emits 1.17 and 1.33 MeV photons. The average energy of 1.25 MeV is used here for a comparison between Si and GaN devices. At that energy, the GaN-to-Si absorption-coefficient ratio is 0.91. This means that depositing 1 rad in a Si device with a specific photon fluence from a Co-60 source will deposit 0.91 rad in a GaN device. That result can also be thought of as 1 rad(GaN) being equivalent to approximately 1.1 rad(Si) for the same Co-60 fluence. For irradiation with 10 keV xrays, comparison of absorption coefficients at that energy yields a GaN-to-Si equilibrium dose ratio of 0.84, which can be expressed as 1 rad(GaN) and 1.19 rad(Si) being equivalent for the same 10 keV xray fluence.

In manmade radiation environments, ionizing-dose-rate effects may be important in specific devices. Evaluating parts for use in such environments involves ground testing at flash xray sources. The corresponding mission radiation requirements are typically expressed as dose rates in units of rad(Si)/sec. For GaN devices, those dose rates must be converted to rad(GaN)/sec to ensure that ground testing is performed to appropriate levels. In general, performing that conversion requires knowledge of the manmade photon environment (energies, fluences) to which devices may be exposed because the mass

energy-absorption coefficient depends on material type and photon energy, especially for relatively low-energy photons.

GaN (and AlGaN and SiC) generate lower transient currents from ionizing radiation dose than Si devices such as MOSFETs of similar size, voltage, and power rating. This is true even though the carrier generation rate for ionizing radiation in GaN is nearly identical to that in Si. Ionizing radiation generates electron-hole pairs in a semiconductor. The rate of generation is proportional to the dose rate in the target semiconductor. The bond-breaking process is a series of events starting with the primary energetic particle that ionizes secondary hot electrons that cause more ionizations in a long series of cascades. Eventually the energies become too low to cause further ionization and are dissipated as heat or phonons. The hot electrons plus the lattice must conserve energy and momentum (Klein, 1968), giving an average ionization energy per generated carrier pair of $E_I = 2.73\ E_g + 0.55$ eV. This is a semi-empirical fit provided by Alig (1975), where E_g is the semiconductor bandgap energy. (This describes a process quite different from optical photo-excitation where the photon energy needed to create a hole-electron pair is essentially E_g.) Since 1 rad is 6.242×10^{11} eV/gm, the carrier generation rate per unit dose rate becomes $6.242\times10^{11}\ \rho / E_I$ (cm^{-3}/sec)/(rads/sec), where ρ is the target semiconductor density. Table G-1 shows some carrier generation rates for various semiconductors. The dose rate (rads/sec) is referenced to the target semiconductor material.

Table G-1. Material Properties and Radiation Carrier Generation Rates of Some Semiconductors

Semiconductor	**Band gap E_g (eV)**	**Energy per ionization E_I (eV)**	**Density (g/cm^3)**	**Generation rate (carrier pairs/cc/sec per rad/sec)**
Si	1.12	3.6	2.33	4.0×10^{11}
GaAs	1.43	4.6	5.32	7.2×10^{11}
GaN	3.41	9.9	6.15	3.9×10^{11}
$Al_{0.3}Ga_{0.7}N$	3.9	11.2	4.9	2.7×10^{11}
4H-SiC	3.21	9.3	3.21	2.2×10^{11}

The carrier generation rates amongst the semiconductors in Table G-1 vary by less than a factor of 3. However, photocurrents in GaN HEMT devices are far less than in Si. Si has an indirect band gap, but the others listed in Table G-1 have direct band gaps. This means that the hole-electron pairs, once they are separated by an electric field, will have a much longer lifetime in Si than in any of the other materials. The reason is because a phonon is needed in Si for the recombination of the hole and electron to take place. Recombination is a statistically rarer in Si, since a free electron first must move within a capture distance of a hole (which is also mobile) or trap (not very mobile); it secondly must emit a phonon having the correct energy. These processes take time to occur, and lifetimes in Si power devices tend to be longer than in GaN HEMTs. Besides the direct bandgap, the defect density in the MOCVD active layers of a HEMT is much higher than in Si. This markedly reduces the lifetimes further. Typical Si power device recombination lifetimes are microseconds to milliseconds, while in GaN HEMT, they are only a few nanoseconds (Gauber, 2017). Comparing a typical Si power MOSFET to a GaN HEMT of similar voltage and current ratings, the HEMT will show 100× less transient "primary photocurrent" for the same dose rate as that for the Si device.

However, charge trapping is another matter. Charge trapping does not occur as readily in a Si device as in a GaN device. The GaN HEMT active layers are already rife with dislocations and traps having densities ranging from 10^6 to 10^9 cm^{-2}. These traps capture some of the radiation-produced electrons. Then the captured electrons are released at a slower rate commensurate with the energy depth of the trap, typically microseconds or milliseconds. While this trapped charge exists, the device characteristics are altered.

Parameters such as the drain on-resistance R_{Don}, the saturated drain current I_{DSS}, or the threshold voltage V_{th} are temporarily but significantly affected by the trapped charges. This effect might be termed "secondary photocurrent" but is actually related to the same trapping phenomena that cause current collapse and pulse instability.

G.3 Dose Enhancement Considerations for GaN Devices

The photoelectric effect produces photoelectrons (or secondary electrons) in a material with an atomic number Z due to the absorption of incident photons with energy E_p. The dependence on Z for the photoelectric effect is often stated in the literature as approximately Z^3, although sometimes as Z^4. The main point is that photoelectron production is a strong function of Z. Compton scattering also produces electrons in an absorbing material, but, in contrast to the photoelectric effect, that process is nearly independent of Z. Whether the photoelectric effect or Compton scattering dominates photon absorption in a given material depends on Z and E_p. For Si (Z = 14), equal interaction cross sections for the two processes occurs at a photon energy of about 70 to 100 keV (i.e., Compton scattering dominates above about 100 keV). For Au (Z = 79), that equality point occurs at $E_p \approx 500$ keV. As an example, for commonly used materials in electronic devices, irradiation using a Co-60 source of gamma rays will produce Compton electrons. In all materials, the photoelectric effect dominates for incident low-energy photons, and Compton scattering dominates for higher-energy photons. The cross-over point depends on the material. (A third effect—electron-positron pair production—becomes important at very high photon energies but is not relevant to the present discussion.)

To describe the main features of the dose enhancement process qualitatively, consider three structures: Au/Si, Au/GaAs, and Au/AlGaN. The atomic numbers (average numbers for GaN and GaAs) and densities for those materials are shown in Table G-2.

Table G-2. Atomic Numbers and Densities for Several Materials Used in Electronic Devices

Material	Atomic Number	Density (g/cm^3)
Si	14	2.33
GaN	19 (average)	6.15
GaAs	32 (average)	5.32
Au	79	19.3
Ga	31	5.91
As	33	5.72
N	7	1.2×10^{-3} (gas)
$Al_{0.3}Ga_{0.7}N$	14.5 (average)	4.9
Al	13	2.70
4H-SiC	9.5 (average)	3.21

To illustrate the concept, consider a 50 keV photon flux incident on the Au side of those three structures so that the photoelectric effect dominates photon absorption in Si, AlGaN, GaAs, and Au. The Au/Si and Au/GaAs structures are considered first. Assuming a Z^3 dependence, then photoelectron production in Au is approximately factors of 180 and 15 more effective than in Si and GaAs, respectively. The "dose enhancement factors" for Au/Si and Au/GaAs are at most 180× and 15×, respectively. The imbalance of photoelectron production at the interface between Au and either of those two materials results in electrons being transported from Au into those materials where they will have a material- and electron-energy-dependent range extending from the interface. Over that range, the excess photoelectrons lose their

energy. That energy deposition process increases the total ionizing dose in the region from the interface to the range of the highest-energy photoelectrons. The deposited dose at any specific distance from the interface depends on the material density, ρ, and the electron energy. In general, the energy deposited per unit path length is given by the product of ρ and IEL, where IEL is the rate of ionizing energy loss (typical units: MeV-cm^2/g). IEL depends on the material and on electron energy. (The energy deposited per unit mass, which is the absorbed dose, is given by the product of IEL and electron fluence.) Thus, the deposited dose from the 50 keV photon flux in the two example semiconductor materials (i.e., Si and GaAs) is enhanced due to the transport of excess secondary electrons generated near the interface in the Au across that interface. The quantitative amount of dose enhancement depends on the Z difference between Au and either of those materials. For example, photoelectrons generated in Si by 50 keV photons will deposit dose in that material, but that dose will be significantly less near the interface than the dose deposited in Si due to excess photoelectrons transported from the Au. In contrast, dose enhancement near the interface will occur in GaAs but will be much less than in the Si case because the Z^3 ratio is significantly lower.

Next consider the case of an Au/AlGaN structure exposed to 50 keV photons. Although Table G-2 lists an average Z for AlGaN, production of photoelectrons in that material will be strongly dominated by Ga atoms (Z = 31). Photoelectron production by nitrogen or aluminum atoms (Z = 7 or 13) is expected to be unimportant due to the assumed Z^3 dependence. On that basis, dose enhancement in the Au/AlGaN case is expected to be more like Au/GaAs than Au/Si since the dominant atomic number in the AlGaN case is nearly the same as the Z for GaAs. A similar situation exists at the interface between the GaN and SiC in GaN HEMTs fabricated on SiC substrates. Dose enhancement near the interface will be greater in the SiC than in the GaN due to the Z^3 ratio; however, it again is more like Au/GaAs than Au/Si. Note also that the distance from the interface over which dose enhancement is important will differ for Si and AlGaN (and GaAs) due to the dependence of deposited dose on material density, which is significantly different for those two materials. Further, the material dependence of IEL at a given electron energy must also be accounted for in a quantitative assessment of dose enhancement.

Now consider a 1 MeV photon flux incident on the above structures so that Compton scattering dominates photon absorption in all four materials. For this case, the dependence of secondary electron production in all of those materials is nearly independent of Z, so the dose enhancement process described above for relatively low-energy xrays is not applicable. That is, dose enhancement is much less important for incident 1 MeV photons. There are electron-scattering differences at interfaces that can result in some dose enhancement, which is at most a factor of two (Dellin, 1974; Long, 1982).

In general, the presence of high-Z materials, such as Au or W or Ta, in a device package or in an integrated circuit itself can cause dose enhancement effects.

A question that arises is whether the procedures used to minimize dose enhancement effects in Si devices during radiation testing for TID effects are also appropriate for GaN devices. In the standard procedure for TID testing of Si devices using a Co-60 source, MIL-STD-883K, Method 1019.9 (2015), it is stated in para. 3.4 “Test specimens shall be enclosed in a Pb/Al container to minimize dose enhancement effects caused by low-energy, scattered radiation. A minimum of 1.5 mm Pb, surrounding an inner shield of at least 0.7 mm Al, is required. This Pb/Al container produces an approximate charged particle equilibrium for Si and for TLDs such as CaF_2. … If it can be demonstrated that low energy scattered radiation is small enough that it will not cause dosimetry errors due to dose enhancement, the Pb/Al container may be omitted.” The use of a high-Z shielding chamber to reduce dose enhancement in Co-60 irradiations by reducing the amount of Compton scatter was examined in (Burke, 1989).

A detailed description by the ASTM of shielding procedures for use in minimizing dose enhancement effects in Si devices during Co-60 irradiations is given in ASTM E1249-15 (2015). In general, an ideal

Co-60 source would emit only 1.17 and 1.33 MeV photons. In practice, however, as noted in ASTM E1249, "Some of the primary Co-60 gamma rays (1.17 and 1.33 MeV) produce lower energy photons by Compton scattering within the Co-60 source structure, within materials that lie between the source and the device under test, and within materials that lie beyond the device but contribute to backscattering. Because of the complexity of these effects, the photon energy spectrum striking the device usually is not well known." In addition, it is mentioned in ASTM E1249 that "shielding materials of tungsten, lead, concrete, or water are often present. Therefore, a significant fraction of the photons incident on the device under test are the result of Compton scattering that produces low energy components in the source output photon energy spectrum. … As an example, the energy spectrum from even a relatively clean Co-60 source has about 35% of its total number of photons with energies of less than 1 MeV (see Garth, 1980)."

To summarize the above shielding discussion, scattering of primary photons in a Co-60 source results in lower-energy photons that may impinge on a device being irradiated. Those photons may then lose their energy by the photoelectric effect instead of by Compton scattering. For that reason, dose enhancement might be significantly increased in a given device structure due to the strong dependence on *Z*. A shielding configuration consisting of Pb/Al is recommended to largely eliminate the lower-energy photons and thereby reduce dose enhancement. The Pb outer layer strongly attenuates those photons, and the Al inner layer serves to eliminate any dose enhancement due to the Pb layer itself (ASTM E1249, 2015).

For radiation testing of non-silicon devices, the ASTM procedure notes the following: "The material of this practice is primarily directed toward silicon based solid state electronic devices. The application of the material and recommendations presented here should be applied to gallium arsenide and other types of devices only with caution." Regarding GaN devices, it seems likely that eliminating lower-energy photons by using a Pb/Al shield during Co-60 testing would also be applicable. The present reasoning is that by largely restricting those photon energies from being incident on a GaN device being irradiated, only Compton scattering will dominate. That is, the photoelectric effect and its associated strong dependence on Z will be avoided. In that situation, dose enhancement effects will be present but minimized, as discussed earlier. Therefore, it is recommended here that a Pb/Al container be utilized in Co-60 TID testing of GaN HEMTs and MMICs. Lower-energy xray sources may also be used with some peril unless dose enhancement effects are considered at the various interfaces.

In general, note that energetic electrons generated by either the photoelectric effect or Compton scattering will be absorbed in both high-*Z* and low-*Z* materials. Those electrons will produce bremsstrahlung xrays as they slow down, which will then deposit an additional ionizing dose in a region that often extends well beyond the range of the electrons themselves.

In addition to the enhancement of TID in irradiated devices, displacement damage enhancement can also occur (Garth, 1985; Meulenberg, 1987). When Compton scattering dominates, such as for shielded Co-60 irradiations, some of the resulting secondary electrons are energetic enough to produce displacement damage. That damage will exhibit a spatial dependence at and near device interfaces. Whether displacement-damage dose enhancement is significant for GaN devices should be given consideration in future work.

G.4 Relative Displacement Damage Sensitivity

Table G-3 shows NIEL values at two incident proton energies for three materials: Si, GaAs, and GaN. Values for Si and GaAs are from Jun (2003); GaN values are from Khanna (2004). NIEL is the rate of nonionizing energy loss per unit distance traveled in a material by the incident energetic particle. Energy loss into nonionizing processes results in the production of displacement damage, which causes changes in the electrical and optical properties of semiconductor materials and devices. The NIEL values shown at

100 MeV indicate that the amount of damage produced is comparable for Si, GaAs, and GaN. However, the relative effectiveness of that damage in altering material and device properties is very different among those materials, with Si being much more sensitive to displacement damage than GaAs and GaN. An example may illustrate one underlying reason for that differing sensitivity. In this example, GaAs and Si are compared; the same reasoning can also be used for GaN since, like GaAs, it is a direct bandgap semiconductor.

Table G-3. Comparison of NIEL Values for 100 and 1000 MeV Protons Incident on Three Materials

Material	**Proton Energy (MeV)**		**Ref.**
	100	1000	
	NIEL (MeV-cm^2/g)		
Si	2.97×10^{-3}	1.34×10^{-3}	Jun (2003)
GaAs	$\sim3.6\times10^{-3}$	$\sim3.5\times10^{-3}$	Jun (2003)
GaN	$\sim3.3\times10^{-3}$	$\sim3.0\times10^{-3}$	Khanna (2003)

Consider the reduction in minority-carrier lifetime in GaAs produced by radiation-induced displacement damage as compared to that occurring in Si. First, the pre-irradiation recombination lifetime in both materials is examined. Silicon is an indirect bandgap material, whereas GaAs (and GaN) is a direct bandgap material. This means that recombination of free carriers (electrons and holes) is an indirect process in Si, which is accompanied by phonon emission (i.e., lattice vibrations). This is a relatively inefficient process, so the resulting minority-carrier lifetime in unirradiated bulk Si is relatively long (i.e., up to 1 msec and longer). In contrast, recombination is a direct process in GaAs (and GaN) that does not involve phonons and is relatively efficient. Pre-irradiation minority-carrier lifetimes are typically less than 100 ns for n- and p-type GaAs for doping concentrations greater than 1×10^{16} cm^{-3} (Jun, 2003). In general, the lifetime in GaAs is a result of three recombination processes: radiative (band-to-band) recombination, Shockley-Read-Hall (SRH) recombination, and Auger recombination. For Si, the carrier lifetime usually is dominated by the SRH process, which involves recombination of carriers at levels introduced in the bandgap. It doesn't take many new defect centers to have an appreciable effect on lifetime in Si since the pre-irradiation lifetime value is so long. In contrast, it takes a relatively large number of radiation-induced recombination centers to affect the carrier lifetime in GaAs via the SRH mechanism since its pre-irradiation value is so short. Now consider the radiative recombination rate in GaAs, which is proportional to the dopant concentration (Brozel, 1996). Carrier removal, which is produced by displacement damage, will effectively reduce, or compensate for, that concentration, which may reduce the radiative recombination rate. However, carrier removal doesn't become significant in GaAs until very large displacement damage doses are deposited. The practical result is that it generally takes significantly more displacement damage dose deposited in GaAs to affect the recombination lifetime significantly compared to Si. Thus, GaAs (and GaN) is expected to be relatively immune to lifetime reduction for most applications.

There appear to be other advantages than just carrier removal with the AlGaN/GaN versus the AlGaAs/GaAs HEMT heterostructure. It has been found that GaN HEMT devices require approximately 10× the displacement damage dose than GaAs HEMTs for the same decrease in DC drain current (Weaver, 2016). Other factors are at work that seem to be improving the immunity of GaN HEMTs to displacement damage. It has been suggested that the larger piezoelectric field at the AlGaN/GaN interface is the reason, giving an added benefit. When displacement damage centers or traps are created, they cause scattering of the carriers in the 2DEG. The large piezoelectric field helps these carriers to be reinjected into the 2DEG channel, thereby mitigating some of the harmful effects of radiation damage. Whether or

not this benefit extends to RF gain or saturated output power in a HEMT or MMIC remains to be seen. More work needs to be done to understand these phenomena more fully.

G.5 Heavy Ion Interactions with GaN HEMT Devices

This section is an attempt to describe some of the main problems and unknowns with GaN HEMTs as they are exposed to the cosmic ray environment in space. The first issue is to try to predict the rate of occurrence of single-event effects (SEE). Heavy-ion (and proton) facilities are used to simulate the cosmic particles. When some simplifying assumptions are made, it is possible to assess the rate of single-event effects in a semiconductor device. The "standard" approximations needed are:

- the single event is triggered by the deposition of a certain critical charge in a well-defined sensitive volume
- the LET (linear energy transfer) of the ionizing particle is constant through the sensitive volume
- a threshold LET is required to deposit enough charge to trigger the event
- the sensitive volume can be approximated by a rectangular parallelpiped (RPP)
- by varying the angle of attack, the path length of the track can be varied, and the critical charge achieved by a lower "effective" threshold LET
- the LET for a given SEE is independent of ion species
- a saturated cross section is observed with sufficient LET

When these approximations are valid, the analysis of the SEE rate can be performed in a straightforward way with knowledge of the particle energy distribution (Peterson, 2011). The particle energy distribution depends upon orbit and the amount of external shielding provided. The approach is especially suited for devices with a well-defined critical charge and a relatively thin, small sensitive volume. Most of the other assumptions naturally fall into place once these two are true. However, in power devices, such as power MOSFETs and likely GaN HEMTs, many of these assumptions may no longer hold.

Of major importance in space missions is to quantify the likelihood of SEB (single-event burnout). SEB in all power semiconductor devices including HEMTs is generally problematic. It appears necessary to derate the peak voltage applied to most power devices significantly as a safety factor against SEB. Some have suggested derating factors of 50% or more. RF power GaN HEMTs seem to have a threshold voltage for burnout, as do many other power devices. The reason usually given for any power device is that the sensitive volume (such as a depletion layer in a Si power device) increases in extent with reverse junction voltage. As charge is deposited in this region, a higher voltage and wider depletion layer will burn out at a lower LET value for the same critical charge. Therefore, the burnout voltage might be expected to vary approximately as $1/\mathrm{LET}^2$, since depletion layer width varies approximately as $V^{1/2}$. Many more complicating factors enter, such as the recombination rate of the ionized charges, the energy deposition density, the spatial variation in electric field and the local temperature rate of rise. Nevertheless, there is a physical reason, however complex, that the SEB voltage should decrease with LET. The approximation that there is a fixed sensitive volume is not necessarily a good one for power devices. There is evidence (Martinez, 2019) that some GaN power switching HEMTs do have a decreasing SEB voltage with LET. It is not yet known if all RF/microwave GaN HEMTs are similar.

In gate oxides of power MOSFETs, the Titus-Wheatley semi-empirical formula (Titus, 1998) for the SEGR (single-event gate rupture) voltage is

$$V_{SEGR} = \frac{E_{BD} t_{ox}}{1 + \frac{Z}{44}} \tag{G-1}$$

where the oxide thickness is t_{ox} (cm), the breakdown field of the oxide is E_{BD} (V/cm), and Z refers to the atomic number of the ionizing species. The SEGR voltage decreases as the atomic number increases for the fixed sensitive volume of the oxide. It would not be surprising if a similar relationship existed in GaN HEMTs, possibly replacing the oxide thickness with the AlGaN barrier thickness. The electric field in the AlGaN has both a lateral and a vertical component at the drain edge of the gate. Therefore, the similarity is imperfect. However, an analogous semi-empirical relationship might nonetheless exist in GaN HEMTs. There is insufficient data currently for such a determination.

It is also known that some GaN power-switching HEMTs have an angular dependence, whereas others do not. The RPP assumption is therefore not always reasonable for the GaN HEMT structure. A strong decrease of the threshold LET for a given drain voltage might indicate that the substrate plays a large role. This is presently unknown. For the typical GaN microwave HEMT, the drain electric field extends far into the substrate, which might explain the angular dependence. If the usual (for GaN HEMTs and MMICs) 4-mil-thick substrate were a significant part of the sensitive volume, the LET for SEB would not be a constant, but would depend upon the energy and position. If the Bragg peak were to fall in the substrate, the standard assumptions would not be valid, and much more complex analyses would be required. Edmonds (2010 & 2012) has provided calculation algorithms for SEE rates with LET varying with position.

Figure G-1 shows some representative SRIM calculations for a simplified stackup of materials that might represent the region of a GaN HEMT at the gate electrode. The gate is assumed to be Au with thin Si_3N_4 passivation. The AlGaN barrier is 25 nm thick, and the GaN buffer is 0.4 um thick, with a SiC substrate 4 mils thick. Note that the x-axis scale is logarithmic to better display the LET values in the layers having widely varying thicknesses and so is grossly out of scale. A stackup of a Si device is also provided for comparison with similar thicknesses, replacing the Au gate with Al, the AlGaN with SiO_2, and the GaN buffer and SiC substrate with Si. Ions of Ar, Kr, and Au with an energy of 15 Mev per nucleon were simulated with SRIM. As can be seen the LETs in the AlGaN and GaN layers are approximately 80% of the LETs in the Si or SiO_2 layers for all the ions. The LETs of the SiC and Si substrates differ little in this example, except for those with Au ions. For the Au ion, the Bragg peak is found about midway into the substrate (as distorted by the log scale). If the sensitive volume were to include the substrate, Au at 15 MeV/u would not be recommended. For planning SEB or SEE tests on GaN HEMTs, it is recommended that an analysis like this one be performed to avoid such difficulties.

One hypothesis to explain the LET dependence of the SEB voltage is as follows. The electric field is highest at the drain edge of the gate. Raising the drain voltage further pushes the device closer to its catastrophic breakdown voltage. When the ion strikes in just the right place, the additional charge initiates the catastrophic breakdown. A lower voltage requires a higher LET depositing more charge to achieve SEB. Once the SEB is initiated, at a small spot along a gate finger, the low impedance of the drain power supply rapidly destroys the device. This hypothesis does not explain why the SEB cross section sometimes is much larger than the geometrical space between source and drain. It does not explain the role of the substrate, which appears to participate in the SEB. Finally, it does not fully explain the fact that the presence of an RF large signal excitation may exacerbate the SEB. Many of these details are currently unknown. For this reason, it is highly recommended that the derating policy for GaN HEMTs in space missions be very conservative. Derating should be based upon thorough heavy-ion test results for SEB. Aggressive derating is not without precedent—consider Si power Schottky diodes that must be derated by more than 50% to protect from SEB.

Another important consideration is the fact in certain power devices such as vertical power MOSFETs, the occurrence of SEB is dependent on not only the voltage but also the ion species for a given LET. This may be understood by the fact that the ion track has some spatial variation or spreading. Charge deposition profiles are not the same with two different ion species having the same LET. This

phenomenon has been observed in SEB in power MOSFETs (Lauenstein, 2011). This is another violation of the standard assumptions, complicating the prediction of SEB rates. It is unknown at this time whether similar ion species dependencies will be found in GaN HEMTs.

Much work needs to be done to settle many of the GaN HEMT SEE issues raised here, which will be accomplished only by future testing and analysis. In doing so, many devices will have to be sacrificed in SEB testing to understand it fully.

The correlation between RF SEB and DC SEB needs much attention. In this guidelines document, DC testing at multiple Q-points has been recommended as a practical way to obtain reliability data. The reliability correlation from DC-to-RF operation is needed for this approach to be valid.

A similar situation exists with SEB. Very little SEB testing has been reported under RF conditions. At this time, the derating of GaN HEMTs for SEB is a major issue for space applications. Until the scope of the problem is better understood, it is recommended that the peak drain voltage be aggressively derated.

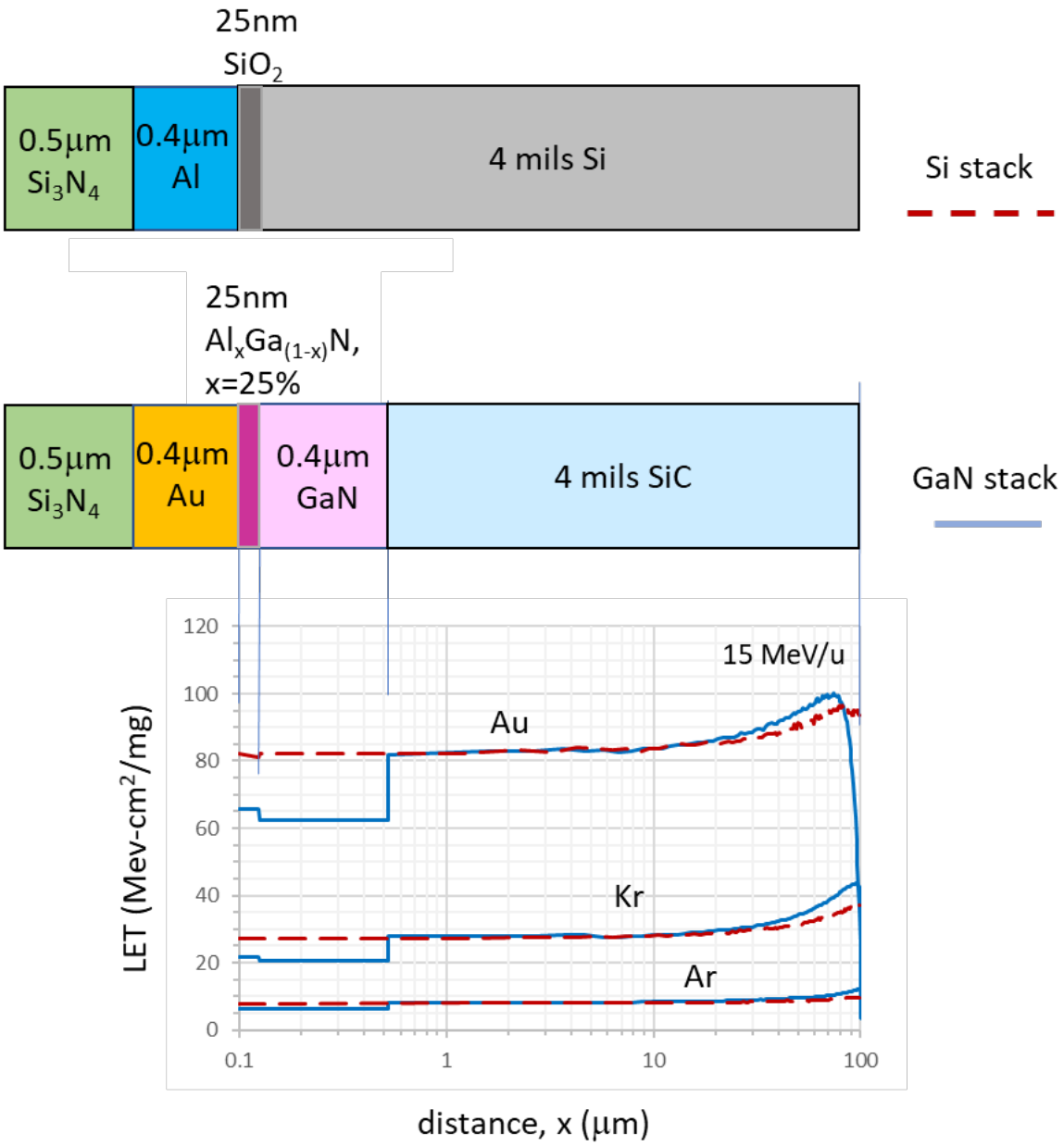


Figure G-1. SRIM™ calculations of LET in a stackup of materials at the gate of a simplified GaN HEMT and a similarly dimensioned Si stackup for comparison. The LETs were computed for an ion energy of 15 MeV/u for Ar, Kr, and Au ions. The x-axis scale is highly distorted (log scale) to show the layers. In the GaN and AlGaN, the LETs for all the ions are about 80% of those in the Si stackup. However, the LETs in Si versus the SiC substrate are very similar. The Bragg peak for the Au ion occurs midway in the SiC substrate, which is an undesirable situation. (SRIM runs kindly performed by Scott Davis, Aerospace.)

Appendix H. Maximum Safe Drain Voltage for Reliable Operation

The purpose of this appendix is to quantify the method for setting a maximum safe drain voltage specification $V_{DSmax.safe}$ for a given reliability requirement. It is recommended that a $V_{DSmax.safe}$ rating be published on a specifications sheet similar to that described in Appendix D, Table D-1. In Section 2 it was suggested that the lower 3σ limit of drain burnout voltage measurements should lie 2× or 3× higher than the specified $V_{DSmax.safe}$ for assurance of reliability. This appendix puts $V_{DSmax.safe}$ on a more rigorous footing once reliability testing has been completed. This is possible once the model coefficients of Eqs. (3-2)–(3-4) have been determined. These equations are proposed reliability models describing a time- and voltage-dependent GaN HEMT failure mode often observed. This mode is not unlike TDDB (time-dependent dielectric breakdown). For these reliability models, the median time to fail becomes voltage dependent above V_{crit}. Assuming that one of these models has been chosen and fit to the reliabilility data, it is now possible to set a value $V_{DSmax.safe}$ that can be guaranteed to meet a specific reliability goal. This appendix shows how to compute this value of $V_{DSmax.safe}$.

For convenience, the three proposed voltage-dependent time-to-failure models are repeated here, along with their example coefficients:

$$t_{50} = A\left(\frac{V_{DS}}{V_{crit}}\right)^{-n} \exp\left(\frac{E_A}{kT}\right) \qquad \text{for } V_{DS} > V_{crit}, \quad \text{V-power} \tag{H-1}$$

$$t_{50} = A\exp\left(\frac{E_A}{kT} + B\left[1-\left(\frac{V_{DS}}{V_{crit}}\right)^{n}\right]\right) \qquad \text{for } V_{DS} > V_{crit} \quad \text{V-exp} \tag{H-2}$$

$$t_{50} = A\exp\left(\frac{E_A - D\left[V_{DS} - V_{crit}\right]^{m}}{kT}\right) \qquad \text{for } V_{DS} > V_{crit} \quad \text{coupled V-exp} \tag{H-3}$$

T_{ch} = 200 °C	mission channel temperature
E_A = 1.4 eV	thermal activation energy
V_{crit} = 25 V	critical voltage
m = 0.4	voltage power coefficient
n = 3	voltage power coefficient
A = 1.5 × 10^{-8} hours	failure time scaling constant
B = 0.2	voltage scaling coefficient
D = 0.025 eV/volts^m	voltage-temperature interaction coefficient
N = 70	total lifetest sample size

As described in Section 3.2, the first model (V-power) has a power law type of voltage dependence, the second (V-exp) an exponential voltage dependence, and the third (coupled V-exp) couples an exponential voltage dependence with temperature. It is assumed that in the process of obtaining the model coefficients for one or the other of these models, a lifetest sample size of N = 70 devices has been used. In these models, as the applied drain voltage is increased, the median time to fail decreases and the reliability is degraded. It is possible to define a value of $V_{DSmax.safe}$ to assure a certain level of reliability for the duration of a given mission. As an example, let the reliability requirement be:

t_m = 15 years (131,486 hours)	mission duration
P_f = 0.3%	probability of failure
C = 90%	confidence factor
T_{ch} = 200 °C	mission usage channel temperature

This states that at the mission channel temperature of 200 °C, there shall be less than 0.3% HEMT failures with 90% confidence by the end of a 15-year mission. The lognormal distribution is assumed first, then the Weibull. Either may be fit to the failure times in most cases.

For the lognormal distribution, the example shape parameter $\sigma = 0.7$ of Section 3.11 is used here for consistency. (Of course the actual shape factor is found by analysis of the lifetest data). Also from Section 3.11, Eqs. (3-8) and (3-9) may be combined and inverted, eliminating $t_{50.LCL}$ to find the needed median time to fail

$$t_{50} = t_m \exp\left(-\sigma\Phi^{-1}\left[P_f\right]\right) - T_{N-1,C-1}\frac{\sigma}{\sqrt{N}} = 9.00\times10^5 \text{ hours} \tag{H-4}$$

where $\Phi^{-1}[P_f]$ is the inverse normal cumulative distribution function for probability P_f and $T_{N-1,\,1-C}$ is the Student's T-statistic as described in Section 3.11. Both $\Phi^{-1}[P_f]$ and $T_{N-1,\,1-C}$ are negative quantities having values –2.748 and –1.294, respectively, in this particular example. This is the needed median time to fail t_{50} in order to achieve the stated reliability goal with the lognormal distribution and sample size assumptions.

A similar calculation can be performed for the Weibull distribution. The example Weibull shape factor $\beta = 3$ of Section 3.11 is used here for consistency (it is of course found from analysis of the lifetest data). Combining Eqs. (3-12) and (3-13), eliminating α_{LCL} and inverting leads to

$$t_{50} = t_m\left(\frac{\chi^2_{N+2,1-C}}{N\left[-\ln\left(1-P_f\right)\right]}\right)^{\frac{1}{\beta}} = 9.83\times10^5 \text{ hours} \tag{H-5}$$

where $\chi^2_{N+2,1-C} = 87.74$ is the chi-square statistic as described in Section 3.11. This median time to fail t_{50} is needed with the assumed Weibull distribution in order to obtain the stated reliability goal.

With these t_{50} values it is possible to determine the maximum allowable value of $V_{DSmax.safe}$. This is done by recasting Eqs. (H-1) through (H-3) for V_{DS} as follows:

$$V_{DS} = V_{crit}\frac{A^{1/n}\exp\left(\dfrac{E_A}{nkT_{ch}}\right)}{t_{50}^{1/n}} \quad \text{V-power} \tag{H-6}$$

$$V_{DS} = V_{crit}\left(1-\frac{\ln\left(t_{50}\right)-\ln\left(A\right)-\dfrac{E_A}{kT_{ch}}}{B}\right)^{1/n} \quad \text{V-exp} \tag{H-7}$$

$$V_{DS} = V_{crit} + \left(\frac{E_A - kT_{ch}\left[\ln(t_{50}) - \ln(A)\right]}{D} \right)^{1/m} \quad \text{coupled V-exp} \qquad \text{(H-8)}$$

and substituting the requisite values of t_{50} commensurate with the reliability requirement for either the lognormal or Weibull distributions from Eqs. (H-4) and (H-5). This gives the values of $V_{DSmax.safe}$ for each assumed model and failure time distribution. The results for the example parameters and assumptions here are shown in Table H-1. Because the example model coefficients were chosen judiciously here, all the values of $V_{DSmax.safe}$ are close to 60 V. In practice, lifetest results should be analyzed in order to obtain the best model and fit it to the data. The lifetesting scheme of Figure 3-3 is recommended for generating the data needed to ascertain the nature of the voltage dependence of the median failure times. The value of $V_{DSmax.safe}$ as obtained here should be published on the rating sheets as recommended in Appendix D. However, the published value of $V_{DSmax.safe}$ should never exceed the 2× to 3× derating from the lower 3σ value of catastrophic breakdown voltage as imposed by the SOA described in Section 2.1.

Note that it is also possible (and has been verified in a few cases) that there may be no real voltage dependence for certain HEMTs and fabrication processes. If so, then the rated $V_{DSmax.safe}$ is no longer limited by a reliability constraint. In this case it is recommended for $V_{DSmax.safe}$ to be 2× to 3× the burnout voltage and/or derated further for single-event burnout (SEB) as needed. However, reliability is still tied to maintaining the channel temperature below the maximum rated value.

The example computations in this appendix suffer from the same limitations as mentioned in Section 3.11, whereby in the inclusion of the confidence factor, it has been assumed that the shape factor for either distribution is known exactly. This is not generally true but can always be verified by performing a sensitivity analysis. By changing the value of shape factor (σ for lognormal or β for Weibull) the change in the resulting $V_{DSmax.safe}$ can be observed. Also it should be mentioned that the values of Table D-1 are similar by virtue of judicious choice of parameters in this example so that the median times to failure t_{50} are about 10^6 hours at a channel temperature of 200 °C and V_{DS} = 60 V. This can be observed in Figure 3-2, where the median times to fail converge at about 60 V. If the reliability requirement is changed to either a more stringent one (lower allowance for probability of failure P_f) or less a stringent one (higher allowance), the needed value of t_{50} would be different. Judging from the curves of Figure 3-2, the values of $V_{DSmax.safe}$ would then become divergent for different models and distributions.

Table H-1. Example Values of $V_{DSmax.safe}$ to Assure Fewer Than 0.3% Failures with 90% Confidence after 15 Years at a Channel Temperature of 200 °C with the Example Model Parameters of Three Model Types and with Lognormal or Weibull Failure Time Distributions

$V_{DSmax.safe}$	Failure time model		
Failure time distribution	Power -V	Exp-V	Coupled exp-V
Lognormal (σ = 0.7)	59.9 V	60.4 V	62.7 V
Weibull (β = 3)	58.1 V	59.8 V	59.7 V

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George Peterson
Air Force Institute of Technology
George.peterson@afit.edu

Ethan Johnson
Air Force Research Laboratory
ethan.johnson.1@us.af.mil

Felix Ejeckam
Akash Systems, Inc.
felix.ejeckam@akashsystems.com

Brian Poling
Air Force Research Laboratory
Brian.poling.2@us.af.mil

Ken Bole
Air Force Research Laboratory
kenneth.bole.2@us.af.mil

Jeanette Quinlan
Akash Systems, Inc.
jeanette.quinlan@akashsystems.com

Christopher Bozada
Air Force Research Laboratory
christopher.bozada@us.af.mil

Steve Tetlak
Air Force Research Laboratory
stephen.tetlak@us.af.mil

Christopher Hay
Analog Devices Inc.
Christopher.Hay@analog.com

Clay Mayberry
Air Force Research Laboratory
clay.mayberry@us.af.mil

Kris Kong
Akash Systems Inc.
kris.kong@akashsystems.com

Tariq Lodhi
Analog Devices Inc.
Tariq.Lodhi@analog.com

Eric Heller
Air Force Research Laboratory
Eric.heller.2@us.af.mil

Brian Loran
Akash Systems, Inc.
brian.loran@akashsystems.com

Uttiya Chowdhury
Bae Systems
uttiya.chowdhury@baesystems.com

Anthony Wilson
Cobham
Anthony.Wilson@cobham.com

Rich Buck
Crane Aerospace
Rich.Buck@craneae.com

Max Zafrani
Freebird Semiconductors
max@freebirdsemi.com

Jim Yount
Cobham
Jim.Yount@cobham.com

Wayne Brown
Crane Aerospace
Wayne.Brown@craneae.com

S.K. Dave Wang
Global Communication Semiconductors, LLC
dwang@gcsincorp.com

Michael Montemayor
Cobham
Michael.Montemayor@cobham.com

Don Gajewski
CREE | Wolfspeed
Don.Gajewski@wolfspeed.com

Bill Cantarini
HiRel Component Solutions, LLC
bcantarini@hirelcomponentsolutions.com

Mike Newman
Cobham
Mike.Newman@cobham.com

Jim Milligan
CREE | Wolfspeed
Jim.Milligan@wolfspeed.com

Shawn Burnham
HR Laboratories
sdburnham@hrl.com

Dave Alexander
COSMIAC
dave.alexander@cosmiac.org ; dralexa@comcast.net

Satyaki Ganguly
CREE | Wolfspeed
Satyaki.ganguly@wolfspeed.com

Abigail Davidson
Ibeos - Formerly Cubic Aerospace
ahd@cubicaerospace.com

Jeff Sanders
Crane Aerospace
jeff.sanders@craneae.com

Alex Lidow
EPC
alex.lidow@epc-co.com

Vernon Harris
Ibeos - Formerly Cubic Aerospace
vernonh@cubicaerospace.com

Khoa Nguyen
Crane Aerospace
Khoa.nguyen@craneae.com

Rob Strittmatter
EPC
robert.strittmatter@epc-co.com

Jonathan Foster
Innoflight, Inc
jfoster@innoflight.com

Gabriele Formicone
Integra Technologies Inc
gformicone@integratech.com
;
GABRIELE.FORMICONE
@asu.edu

Dan Sullivan
KCB Solutions
dsullivan@kcbsolutions.com

Mike Gumino
Lockheed Martin Space
mike.gumino@lmco.com

Sultan Lilani
Integra Technologies Inc
Sultan.Lilani@integra-
tech.com

Masaya Iwamoto
Keysight
masaya_iwamoto@keysight.c
om

Rob Hodge
Lockheed Martin Space
rob.hodge@lmco.com

Doug Sheldon
Jet Propulsion Laboratory,
California Institute of
Technology
douglas.j.sheldon@jpl.nasa.g
ov

Jan J. Zygmaniak
L3Harris Technologies
jan.zygmaniak@l3harris.com

Stanley Schwartz
Lockheed Martin Space
stanley.w.schwartz@lmco.co
m

Leif Scheick
Jet Propulsion Laboratory,
California Institute of
Technology
leif.z.scheick@jpl.nasa.gov

Phil Smith
L3Harris Technologies
phil.p.smith@L3Harris.com

Peter Ersland
MACOM Technology
Solutions
peter.ersland@macom.com

Michael Han
Jet Propulsion Laboratory,
California Institute of
Technology
michael.han@jpl.nasa.gov

M. Amimul Ihsan
Lockheed Martin Space
muhammad.a.ihsan@lmco.co
m

Jonny Pellish
NASA
jonathan.pellish@nasa.gov

Scott Gore
Jet Propulsion Laboratory,
California Institute of
Technology
scott.h.gore@jpl.nasa.gov

Manuel Rossy
Lockheed Martin Space
manuel.rossy@lmco.com

Kenneth LaBel
NASA
kenneth.a.label@nasa.gov

Ted Apple
Jet Propulsion Laboratory,
California Institute of
Technology
ted.apple@jpl.nasa.gov;
tedappleeee@gmail.com

Matt Sauer
Lockheed Martin Space
Matthew.a.sauer@lmco.com

Jean-Marie Lauenstein
NASA GSFC
jean.m.lauenstein@nasa.gov

Jason Osheroff
NASA Science Systems Applications, Inc.
jason.m.osheroff@nasa.gov

Ioulia Smorchkova
Northrop Grumman
Ioulia.smorchkova@ngc.com

Ken Decker
Qorvo
kenneth.decker@qorvo.com

Aditya Gupta
Northrop Grumman
Aditya.Gupta@ngc.com

Jim Oliver
Northrop Grumman
j.oliver@ngc.com

Abbas Torabi
Raytheon
atorabi@Raytheon.com ; Bluephoton@verizon.net

Andy Moor
Northrop Grumman
Andrew.moor@ngc.com

Mike Wojtowicz
Northrop Grumman
mike.wojtowicz@ngc.com

Bill Rowe
Raytheon
William.J.Rowe@raytheon.com

Ben Heying
Northrop Grumman
benjamin.heying@ngc.com

Patrick Shea
Northrop Grumman
patrick.shea@ngc.com

David Drapeau
Raytheon
David.J.Drapeau-nr@raytheon.com

Carolina Alaniz
Northrop Grumman
carolina.alaniz@ngc.com

Ron Hardesty
Northrop Grumman
Ronald.Hardesty@ngc.com

Helen Ying
Raytheon
Helen.Ying@raytheon.com

Dario Buttari
Northrop Grumman
Dario.buttari@ngc.com

Wen-Ben Luo
Northrop Grumman
Wen-Ben.Luo@ngc.com

Kurt Ketola
Raytheon
ketola@raytheon.com

David Eng
Northrop Grumman
david.eng@ngc.com

Gergana Drandova
Qorvo
Gergana.Drandova@Qorvo.com

Nick Kolias
Raytheon
Nicholas_J_Kolias@raytheon.com

Pierre Hilaire
Raytheon
Pierre.R.Hilaire@raytheon.com

Ashley Wenger
The Boeing Company
Ashley.N.Wenger@boeing.com

Nick Rosales
The Boeing Company
nicholas.p.rosales@boeing.com

Rob Leoni
Raytheon
Robert_E_Leoni@raytheon.com

Chahriar Assad
The Boeing Company
chahriar.assad@boeing.com

Nicole Carpentier
The Boeing Company
nicole.a.carpentier@boeing.com

Stephen Jakubowski
Raytheon
stephen.e.jakubowski@raytheon.com

Jason Douglas
The Boeing Company
jason.e.douglas@boeing.com

Rodrigo Deleon
The Boeing Company
rodrigo.deleon@boeing.com

Chris Wiggins
Sumitomo Electric Device Innovations USA, Inc.
cwiggins@sei-device.com

John Grebliunas
The Boeing Company
john.r.grebliunas@boeing.com

Serop Koushinian
The Boeing Company
serop.koushinian@boeing.com

Mikiharu Ohoka
Sumitomo Electric Device Innovations USA, Inc.
mohoka@sei-device.com

Karim Boutros
The Boeing Company
karim.s.boutros@boeing.com

Shengyi Liu
The Boeing Company
Shengyi.Liu@boeing.com

Paul Patterson
Sumitomo Electric Device Innovations USA, Inc.
ppatterson@sei-device.com

Lilian Hanna
The Boeing Company
Lilian.Hanna@boeing.com

Stella Kim
The Boeing Company
stella.k.kim@boeing.com

Javier Valle
Texas Instruments
jvalle@ti.com

Martin Hummel
The Boeing Company
martin.e.hummel@boeing.com

Stephanie Alberty
The Boeing Company
stephanie.p.alberty@boeing.com

Stephen Thomas III
The Boeing Company
stephen.thomas-iii@boeing.com

Dan Sable
VPT Inc.
sable@vptpower.com

Rajesh Mongia
ENGIN-IC
rajesh.mongia@engin-ic.com

Tae Roh
The Boeing Company
Tae.J.Roh@boeing.com

David Reusch
VPT Inc.
dreusch@vptpower.com

Andrew Popp
Infineon
Andrew.Popp@infineon.com

Thomas Rust-III
The Boeing Company
thomas.rust-iii@boeing.com

Eliashevich, Ivan
WIN
ieliashevich@use.winfoundry.com

Chris Hart
Infineon
Chris.Hart@infineon.com

Timothy Lee
The Boeing Company
timothy.t.lee@boeing.com

Everett Cole
Analog Devices Inc.
Everett.Cole@analog.com

Odile Ronat
Infineon
Odile.Ronat@infineon.com

Zenon Carlos
The Boeing Company
zenon.f.carlos@boeing.com

Everett Cole
Analog Devices Inc.
everettc3@icloud.com

Tiger Liu
Infineon
Tiger.Liu@infineon.com

Tom Green
TJ Green Associates, LLC
tgreen@tjgreenllc.com

Efi Ojalvo
ELTA Systems Ltd.
eojalvo@elta.co.il

Shunhe Xiong
IR HiRel, An Infineon Technologies Company
Shunhe.xiong@infineon.com

Kurt Smith
Visic Technologies
kurt@visic-tech.com

Yaron Knafo
ELTA Systems Ltd.
knafoy@elta.co.il

Ndiogou Wack Diongue
Macdonald, Dettwiler And Associates Corporation
ndiogou-wack.diongue@mdacorporation.com

Bill Cox
Maxar
william.cox@maxar.com

Roy Andrada
Maxar
Roy.Andrada@maxar.com

Bill Cox
Maxar
William.Cox@sslmda.com

Jim Vinson
Renesas Electronics
jim.vinson.vz@gr.renesas.com

Catherine Keys
Maxar
Catherine.Keys@maxar.com

Kat Kasim
The Boeing Company
Kawthar.Kasim@boeing.com

Jim Loman
Maxar
james.loman@sslmda.com

Kat Kasim
The Boeing Company
kawthar@gmail.com

John Walker
Maxar
JohnF.Walker@maxar.com

Art Witulski
Vanderbilt
arthur.f.witulski@vanderbilt.edu

Ron Remba
Maxar
Ronald.Remba@maxar.com

Mike McCurdy
Vanderbilt
mike.mccurdy@Vanderbilt.Edu

Ron Remba
Maxar
Ronald.Remba@sslmda.com

APPROVED BY_____ DATE_____
(AF OFFICE)